

Clock and Data Recovery for Serial Digital Communication

focusing on bang-bang loop CDR design methodology

ISSCC Short Course, February 2002

Rick Walker

Agilent Laboratories

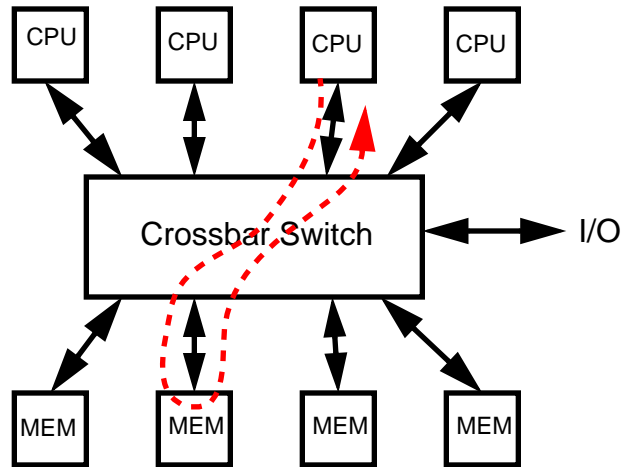
Palo Alto, California

rick_walker@labs.agilent.com

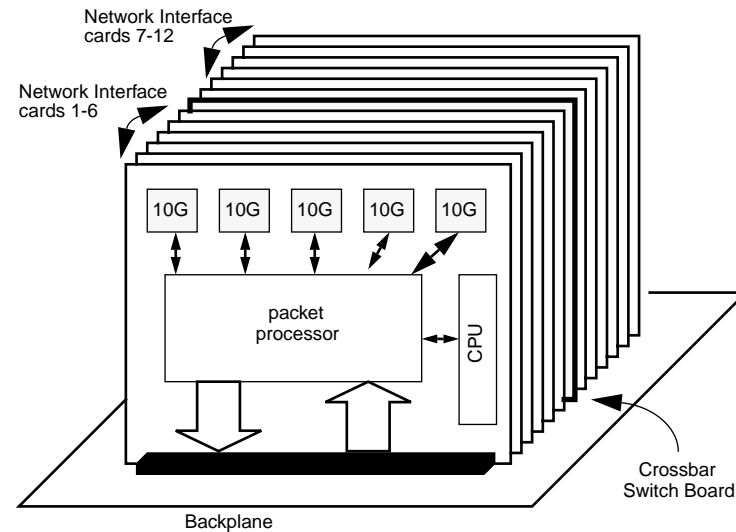
Outline

- Overview of serial data communications
 - Degradation mechanisms, data coding
 - Jitter measurements
- Clock recovery methods
 - Linear PLL review and components
 - BB PLL theory

Diversity of CDR applications



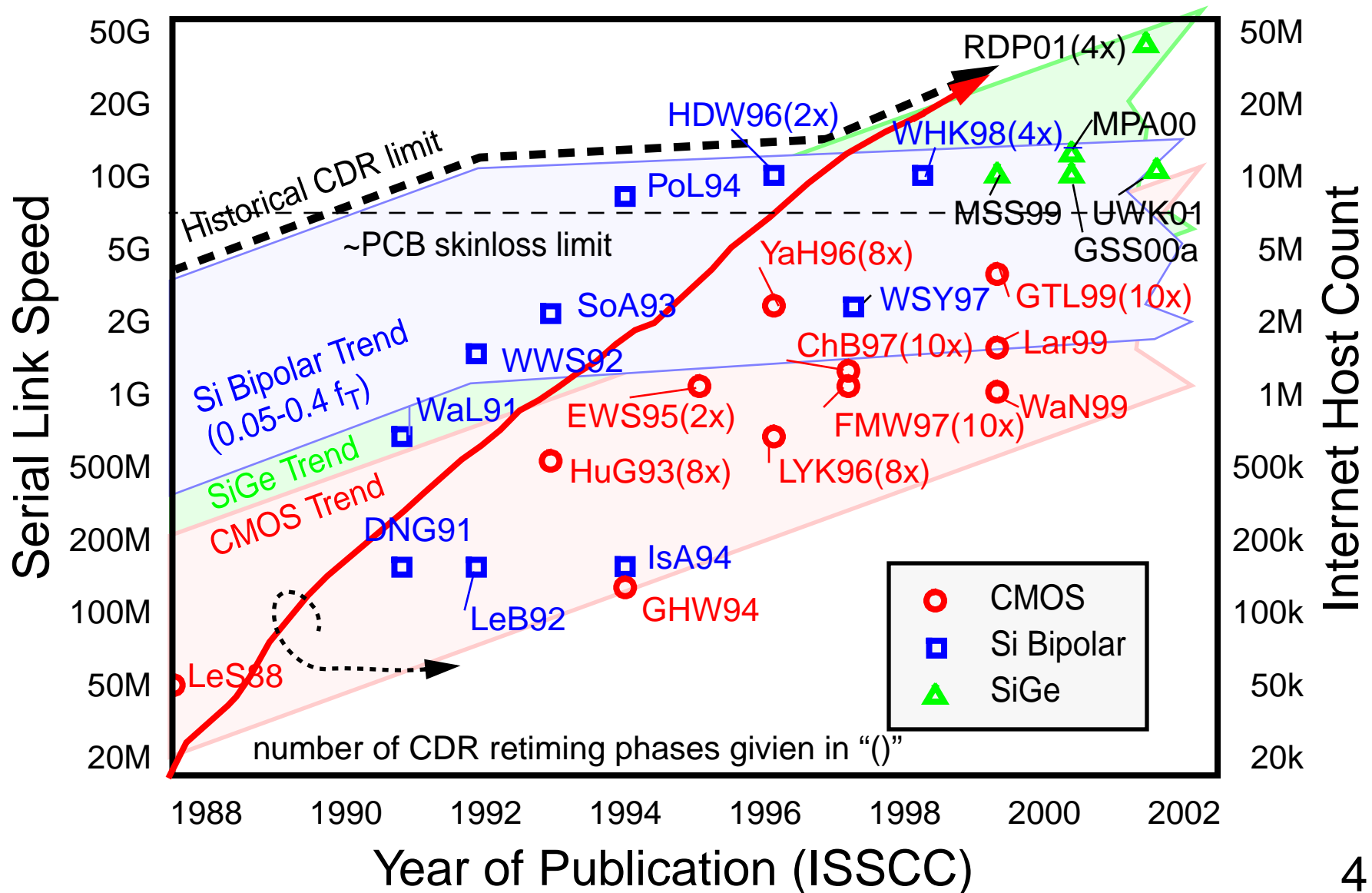
Linecard to Router



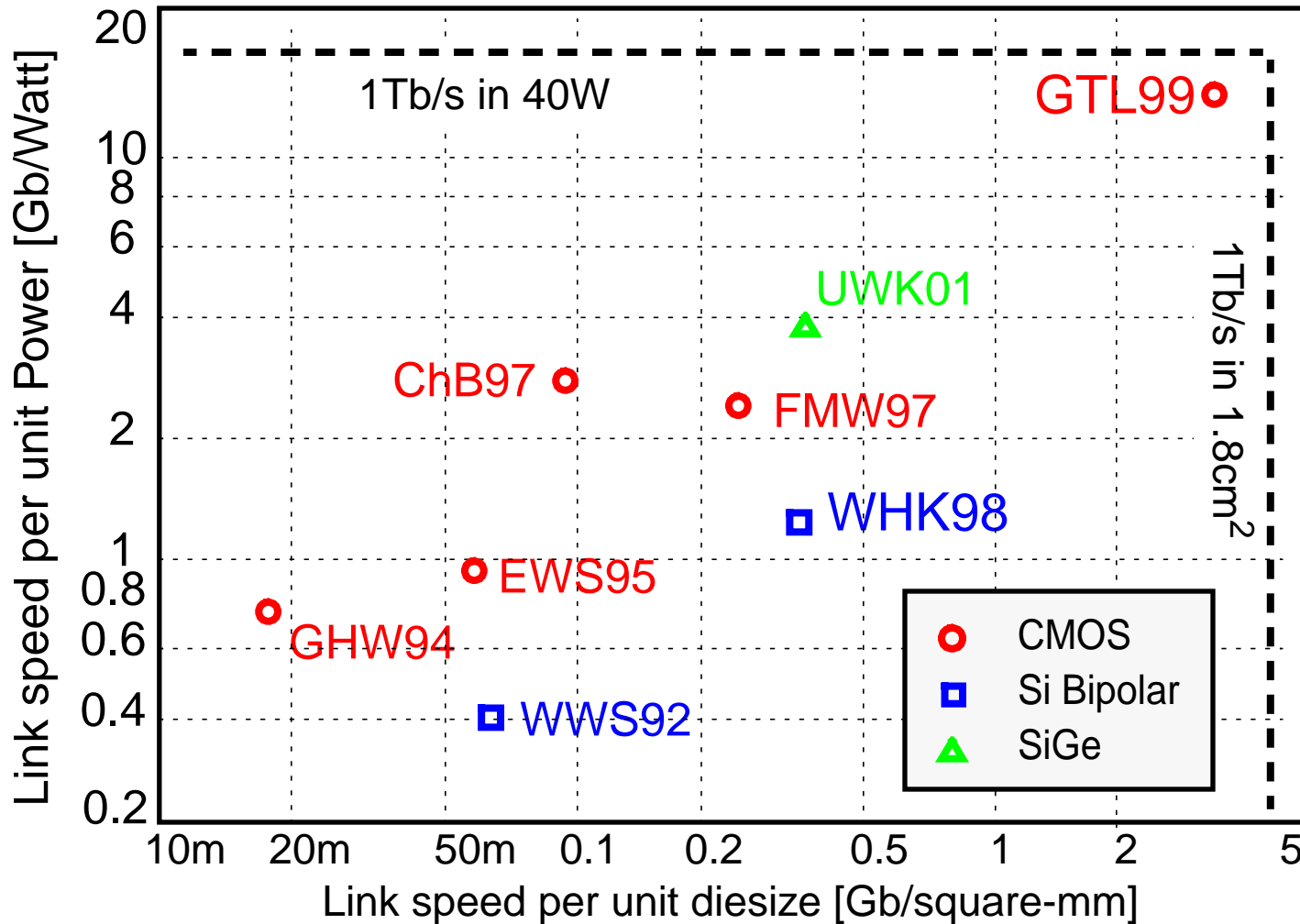
CPU-CPU/Memory

- Clock and Data Recovery applications span the range from high-volume, low-cost datacom applications to high-performance, long-haul telecom applications
- Many different trade-offs tailor each circuit to the target

CDR data rates over time



TX/RX Gb/W and Gb/mm²

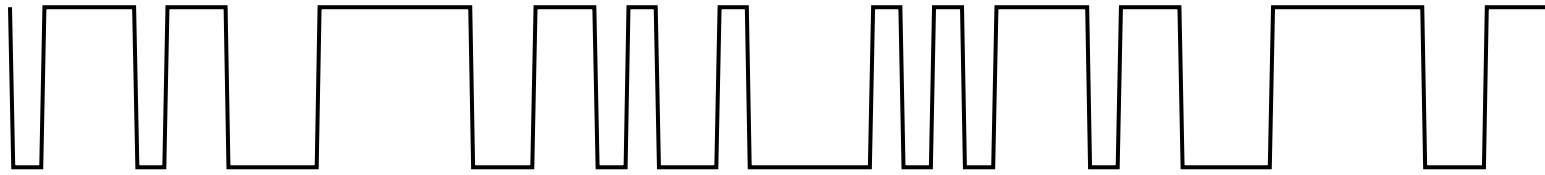


Circuit power and die size can be system-limiting factors. Gb/W and Gb/mm² are plotted for complete TX/RX designs published between ISSCC'92 and 2001. Dashed lines represent an aggressive chip supporting 1Tb/s in a total of 40W and 1.8cm². 5

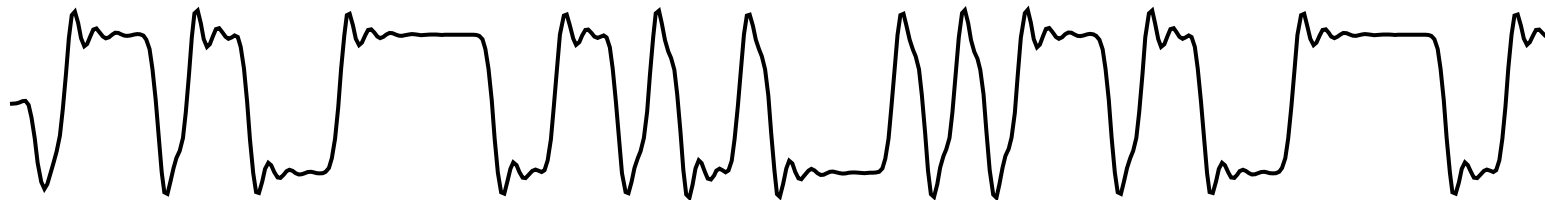
Basic Idea

Serial data transmission sends binary bits of information as a series of optical or electrical pulses:

0111011000111110011010010000101011101100011111..



The transmission channel (coax, radio, fiber) generally distorts the signal in various ways:



From this signal we must recover both clock and data

Some Signal Degradation Mechanisms

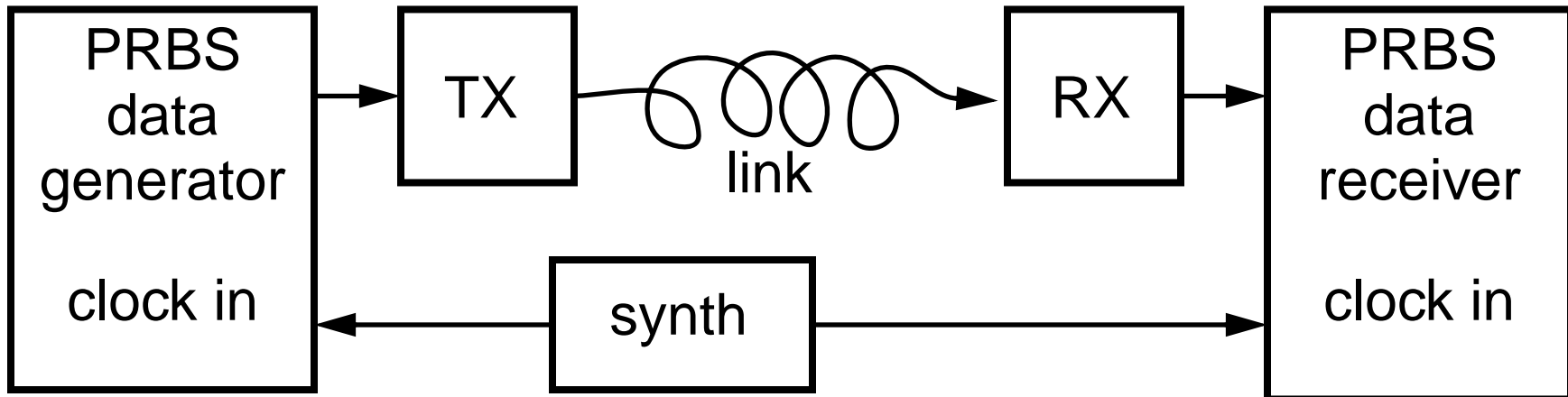
- AC coupling droop, baseline wander
- Optical pulse dispersion
- Skin / dielectric loss [YFW82, WWS92, FMW97]
- Random noise
- E+O crosstalk
- Intersymbol interference
- Connector discontinuities

Coding for Desirable Properties

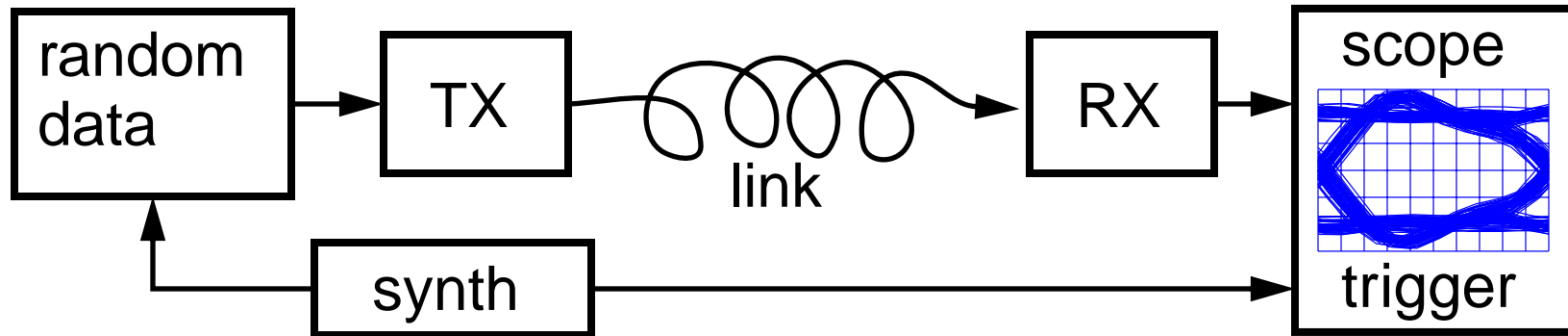
- DC balance, low disparity
- Bounded run length
- High Coding Efficiency
- Spectral Shaping (eg: reduce BW or DC component)
- *Many Variations are Possible!*
 - Manchester [San82]
 - mB/nB [Gri69][Rou76][WiF83] [YKI84] [Pet88]
 - Scrambling: SONET, 64b/66b [CCI90]
 - CIMT [WHY91], Conservative Code [Ofe89]

Bit Error Rate (BER) Testing

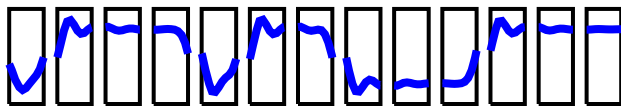
- Pseudo-Random-Bit-Sequence (PRBS) is used to simulate random data for transmission across the link
- PRBS pattern 2^N-1 Bits long contains *all* N-bit patterns
- Number of errored-bits divided by total bits = BER.
- Typical links are designed for BERs better than 10^{-12}



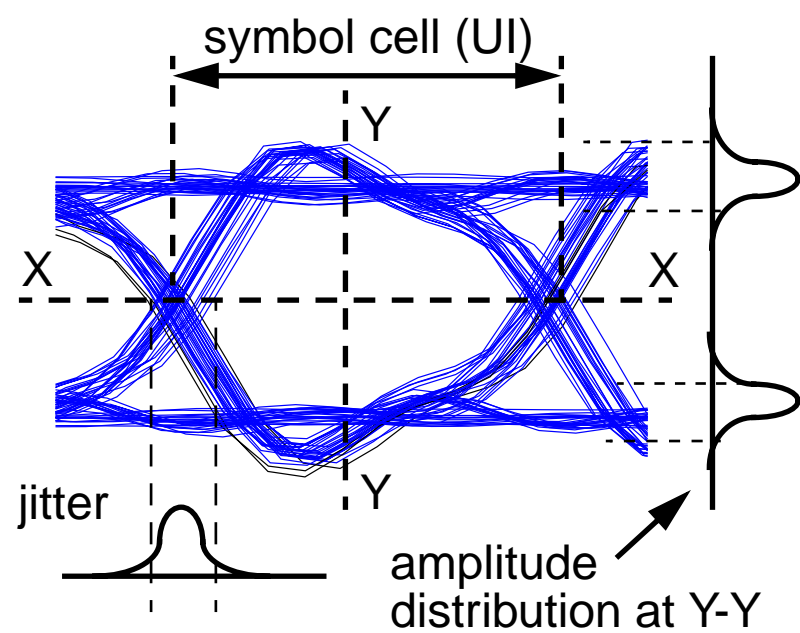
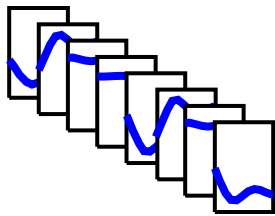
Eye diagram construction



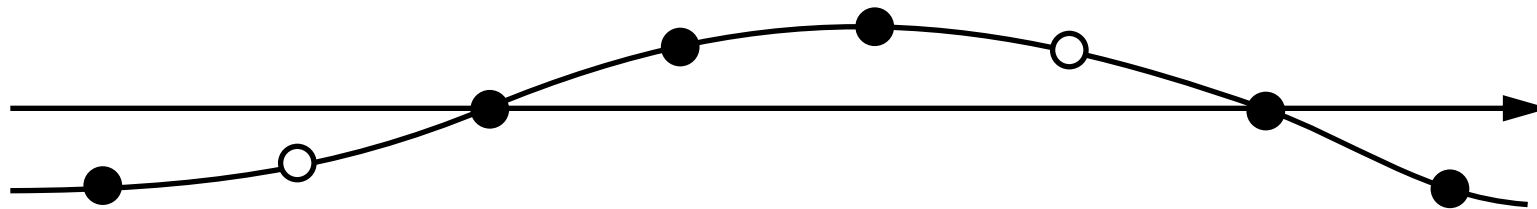
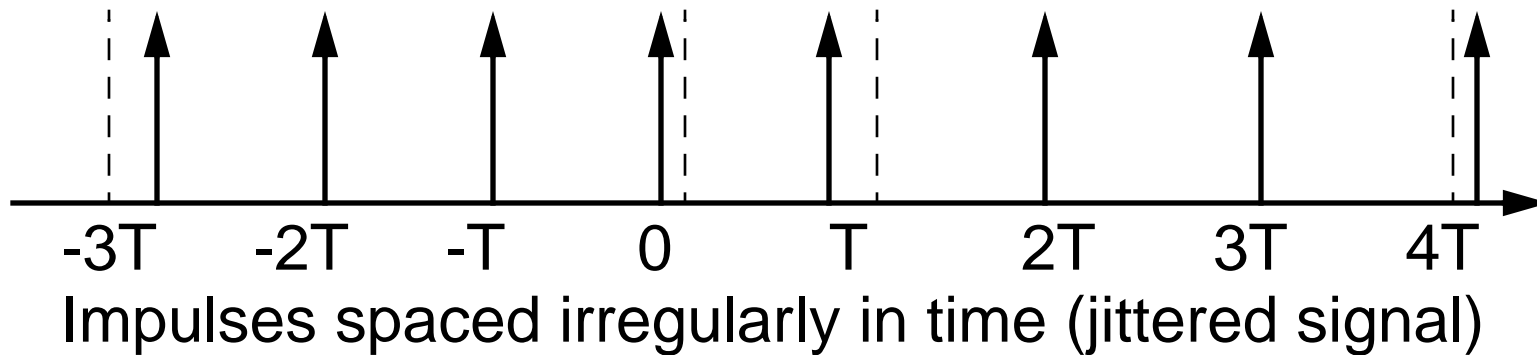
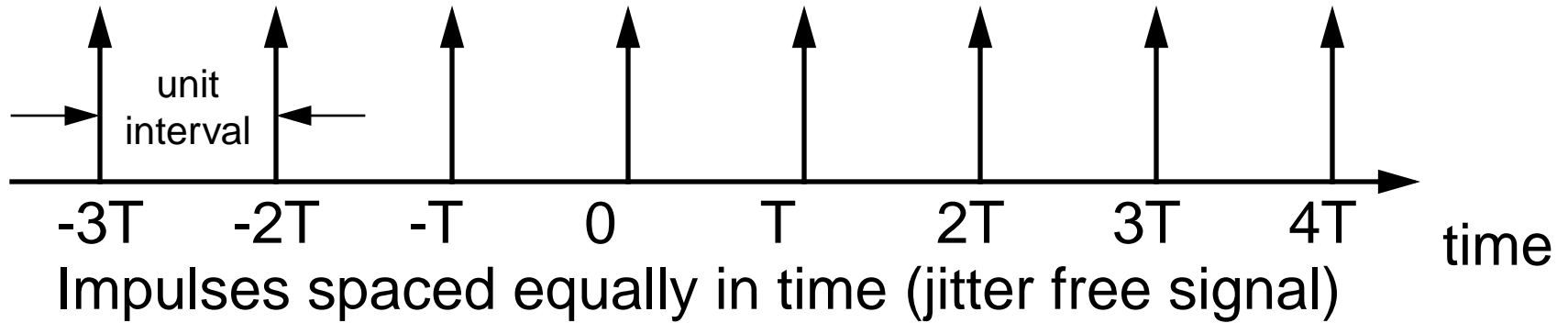
Use a precise clock to chop the data into equal periods



overlay each period onto one plot



Definition of Jitter



Errors treated as discrete samples of continuous time jitter

Jitter Measurements

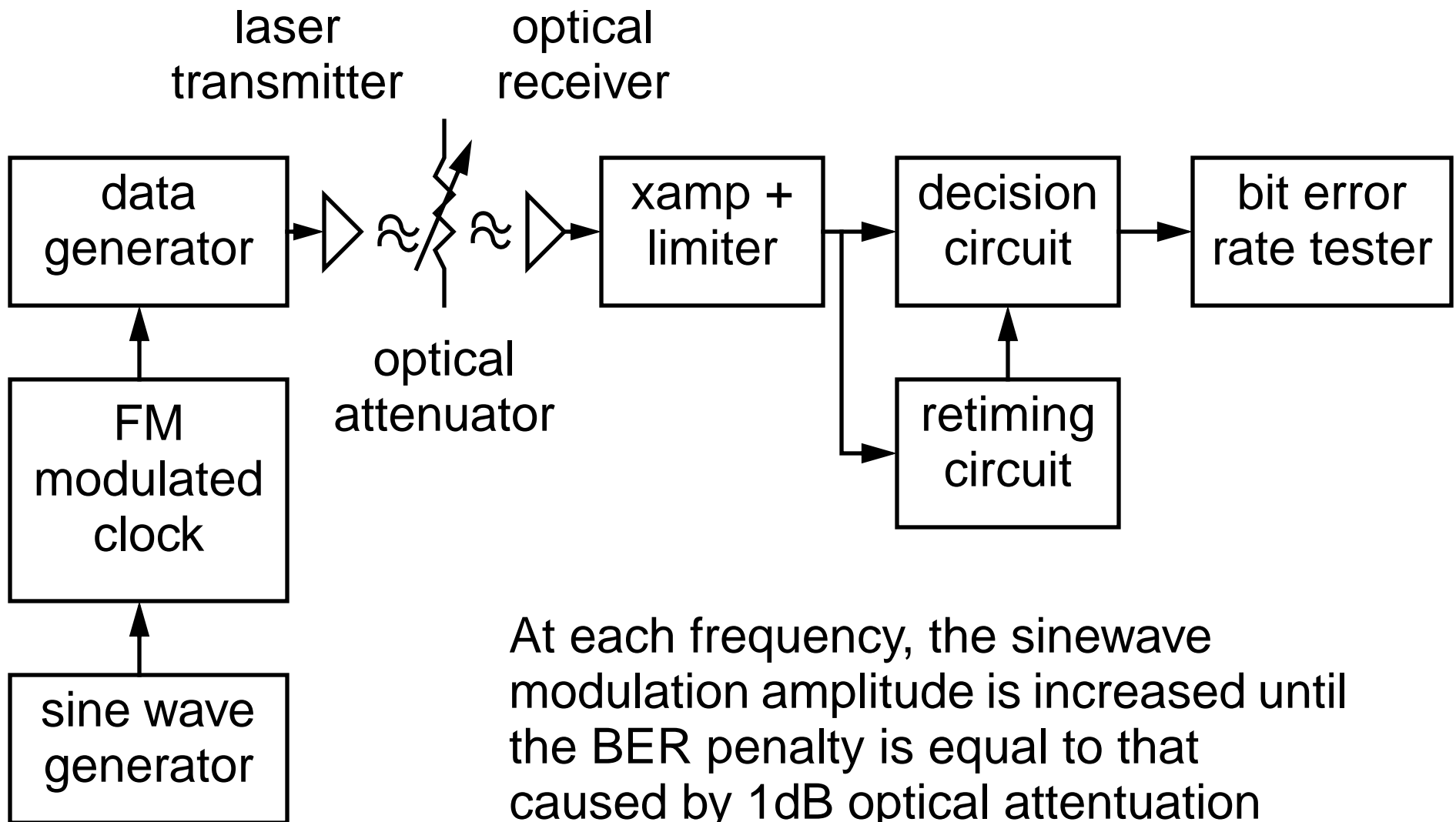
Jitter Measurements

- *Datacom Style:* Ethernet + Fiber Channel
based on time-domain eye diagrams
 - Deterministic Jitter
 - Random Jitter
- *Telecom Style:* SONET
based on frequency-domain jitter spectrums
 - Jitter Tolerance
 - Jitter Transfer
 - Jitter Generation

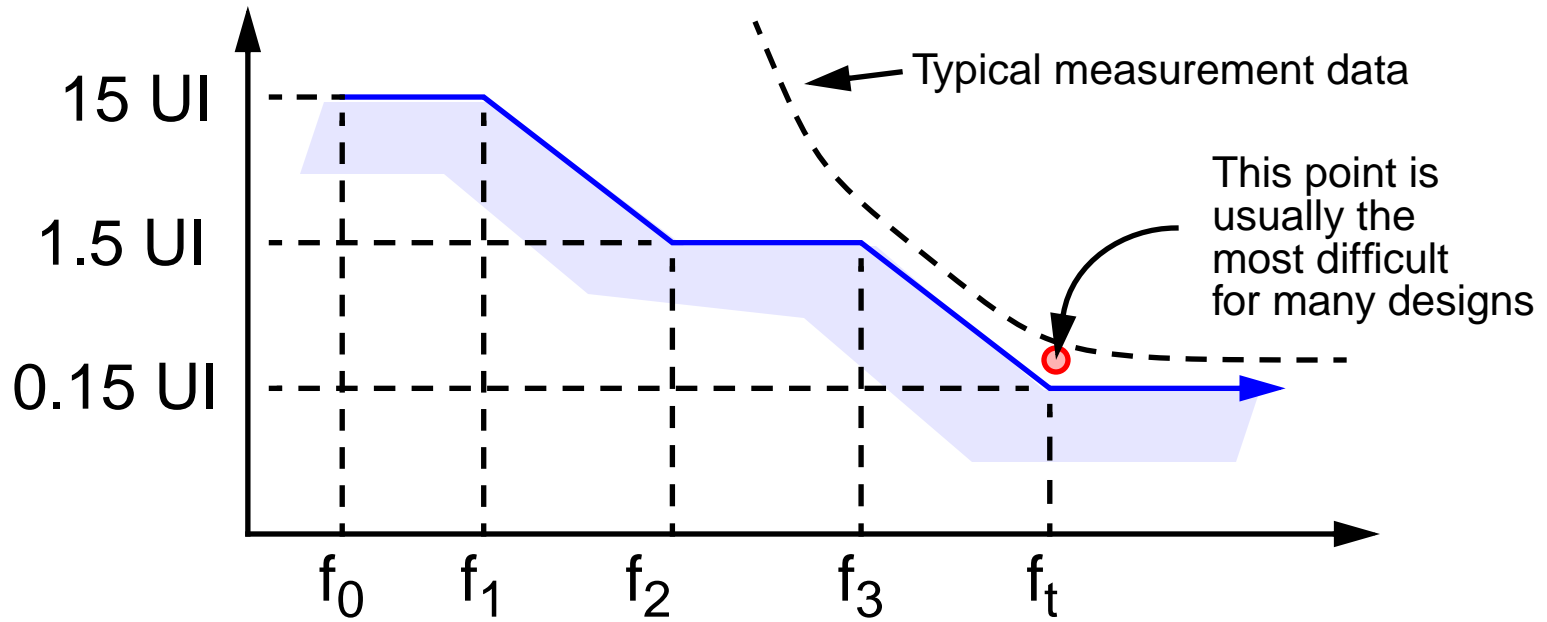
Deterministic and Random Jitter

- Random Jitter (RJ)
 - data source is simple repetitive “clock-like” pattern.
 - RMS jitter is measured at zero crossings of eye-diagram
 - measured jitter is mostly due to clock noise
- Deterministic Jitter (DJ)
 - data source is complex scrambled data
 - pk/pk jitter is measured at zero crossings of eye-diagram
 - RJ contribution is subtracted from the measurement
 - measured jitter is mostly due to bandwidth limitations in the data path.

Jitter Tolerance Test Setup

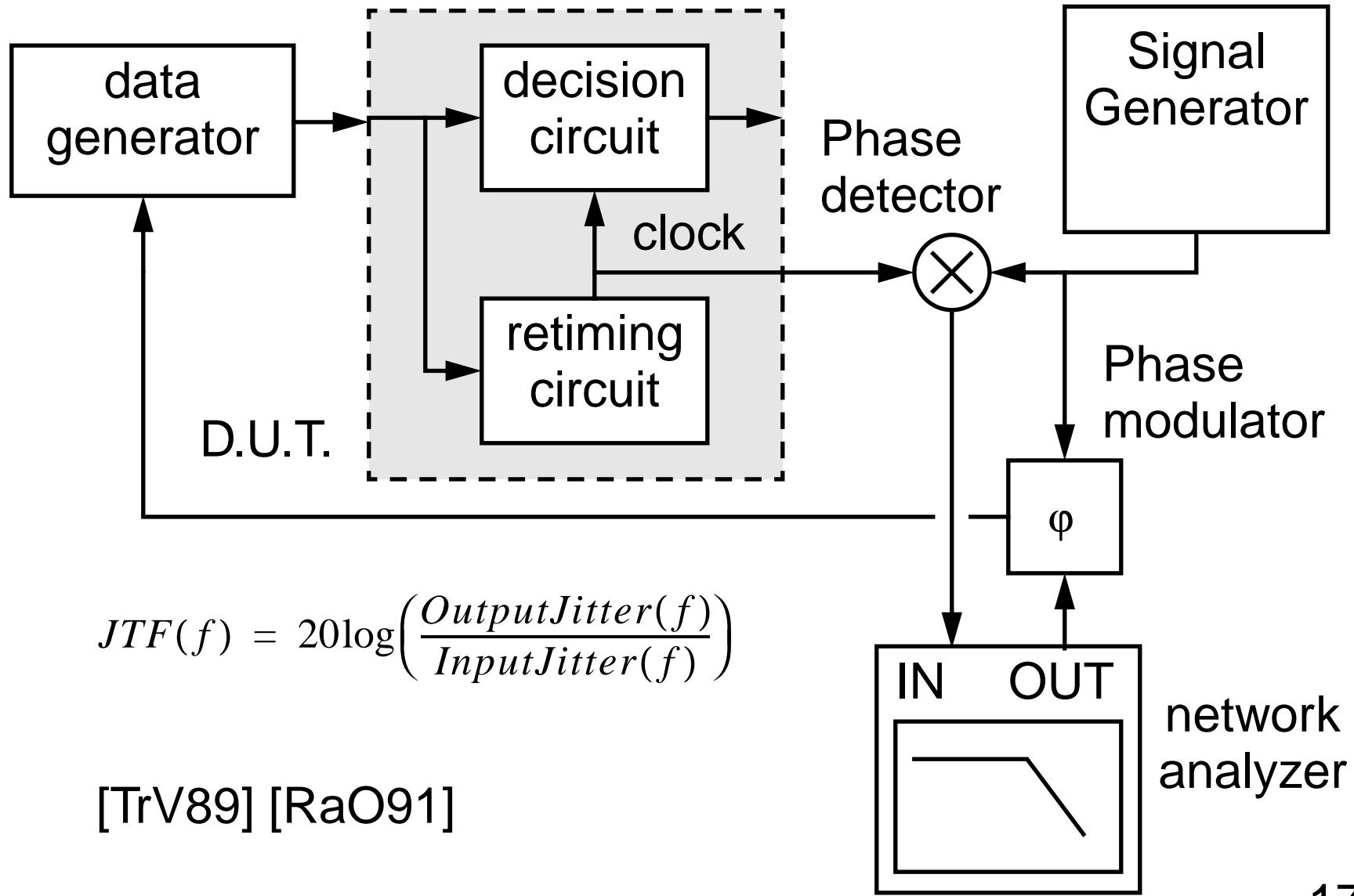


SONET Jitter Tolerance Mask



Data Rate		f_0 [Hz]	f_1 [Hz]	f_2 [Hz]	f_3 [kHz]	f_t [kHz]
OC-3	155 Mb	10	30	300	6.5	65
OC-12	622 Mb	10	30	300	25	250
OC-48	2.488 Gb	10	600	6000	100	1000
OC-192	10 Gb	10	2400	24000	400	4000

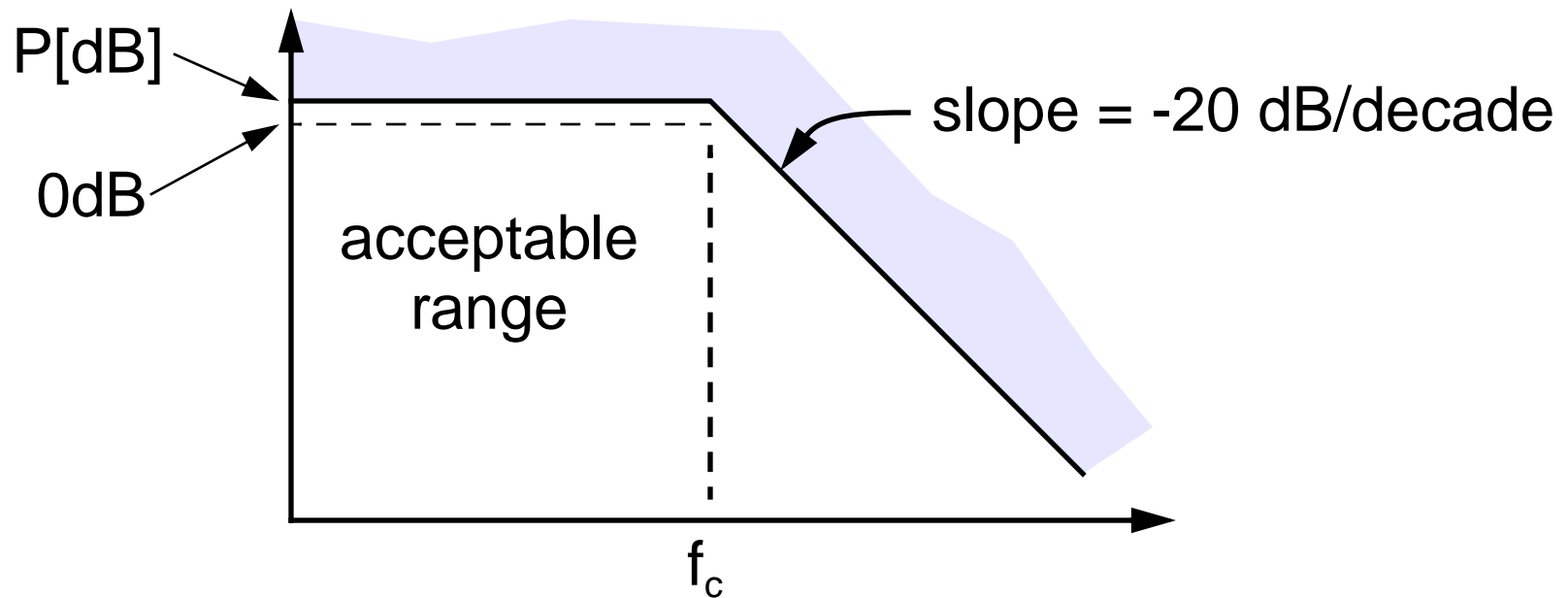
Jitter Transfer Measurement



$$JTF(f) = 20\log\left(\frac{OutputJitter(f)}{InputJitter(f)}\right)$$

[TrV89] [RaO91]

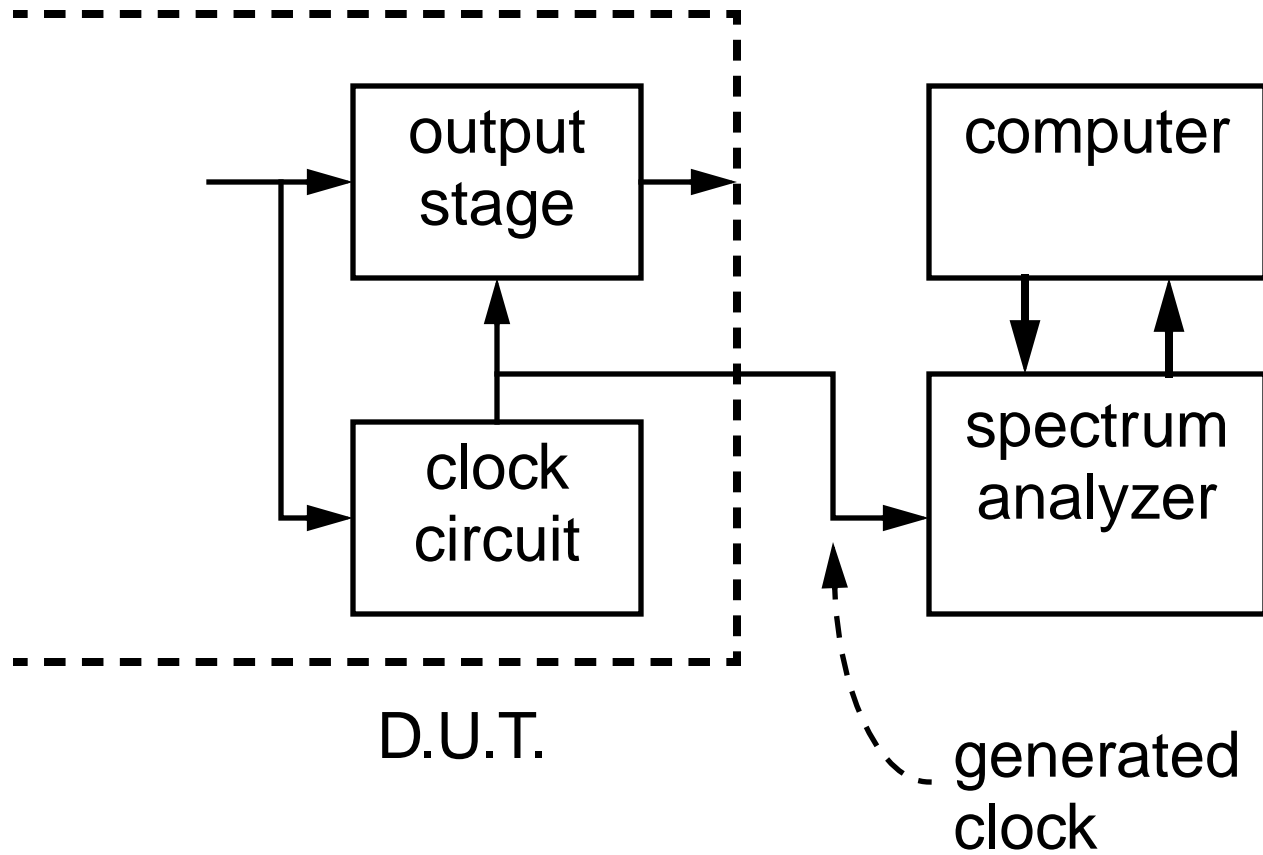
Jitter Transfer Specification



Data Rate	f_c [kHz]	P [dB]
155 Mb	130	0.1
622 Mb	500	0.1
2.488 Gb	2000	0.1

This specification is intended to control jitter peaking in long repeater chains

Jitter Generation



Jitter Generation (cont.)

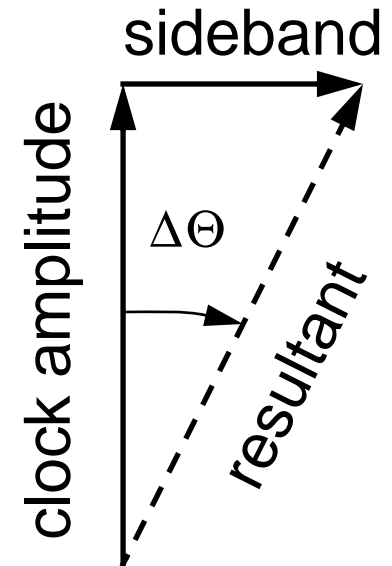
1) Measure Jitter Sidebands around Clock

$$Jitter_{pp(rads)} = 2\Delta\Theta \cong 2 \operatorname{atan}\left(\frac{V_{sideband}}{V_{clock}}\right)$$

2) Multiply Jitter components by Filter Mask

3) RMS sum total noise voltages over band

4) Convert RMS noise voltage to RMS jitter

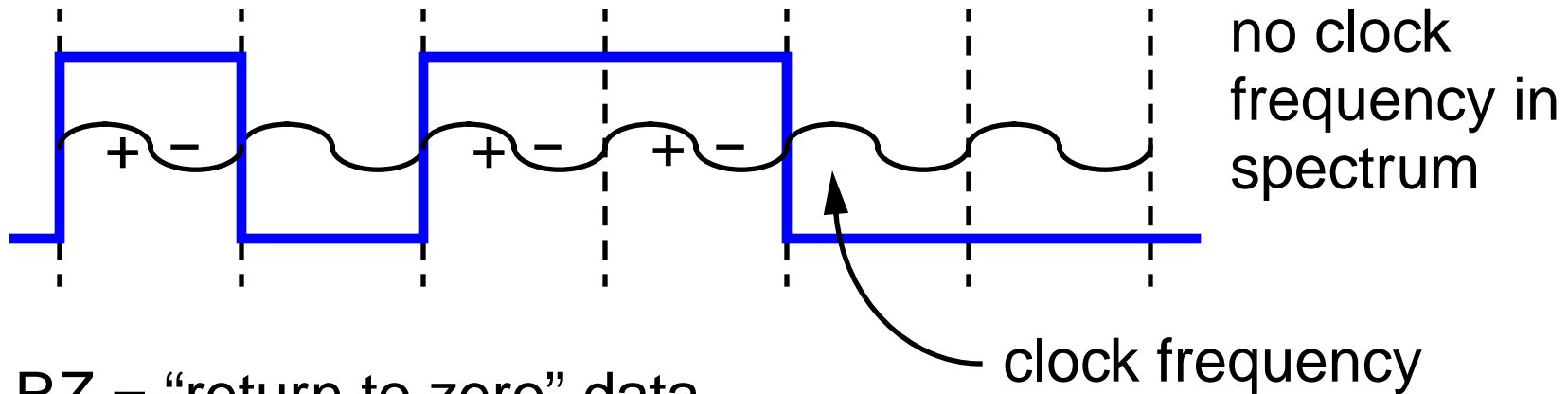


OC-48 (2.488 Gb/s SONET) specifies 12 kHz hipass filter, and maximum 0.01 UI RMS integrated jitter.

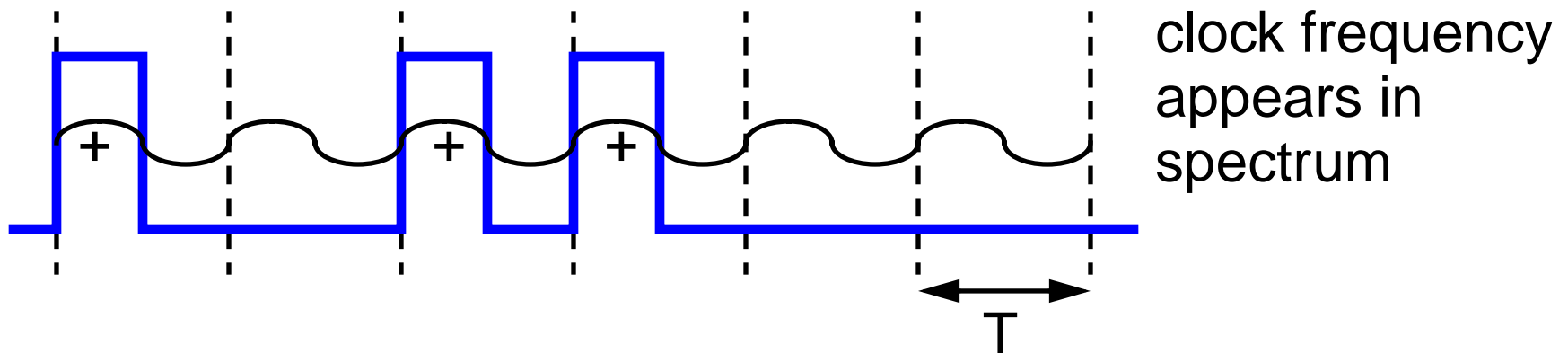
Clock Recovery Concepts

NRZ and RZ signalling

NRZ = "non return to zero" data

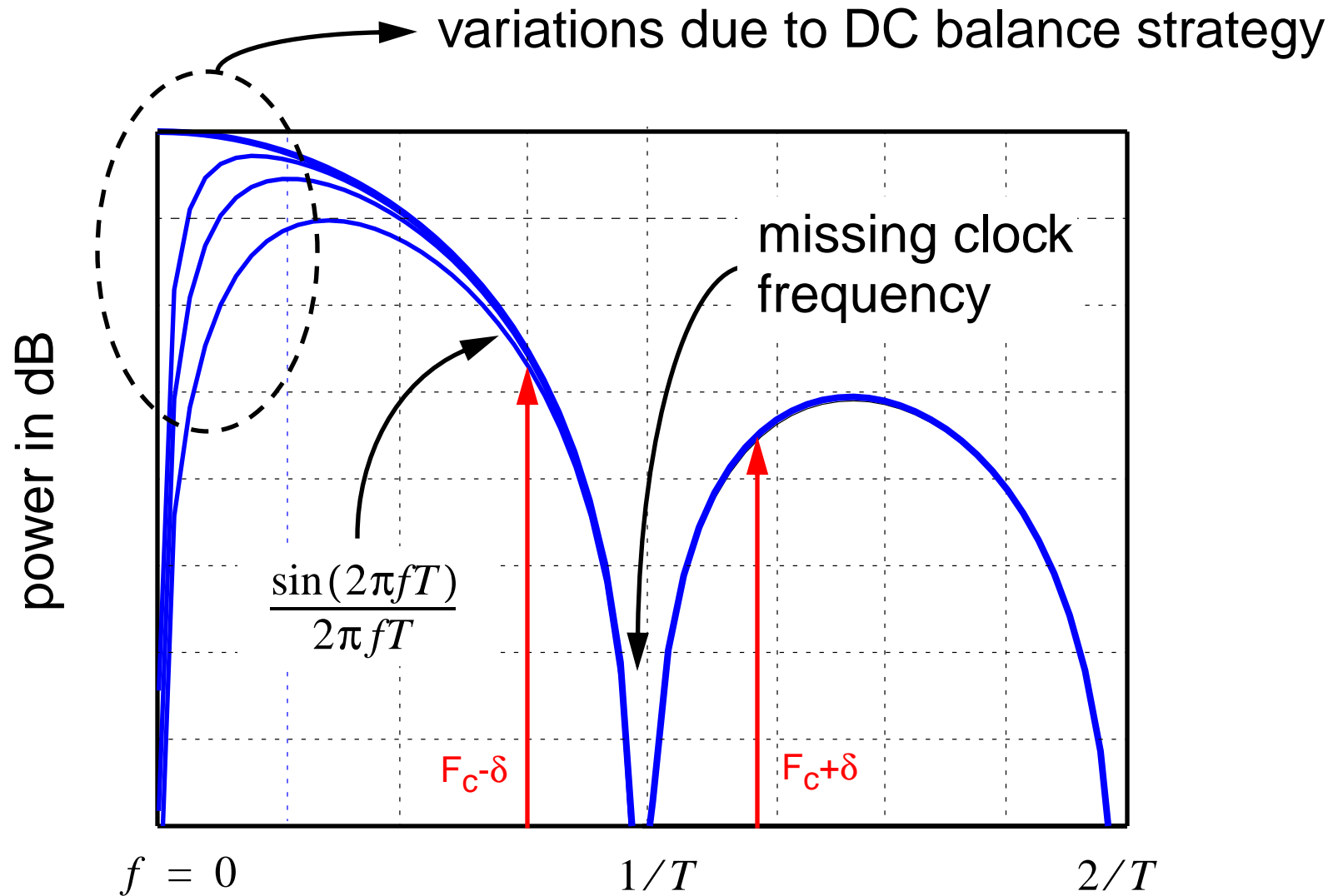


RZ = "return to zero" data

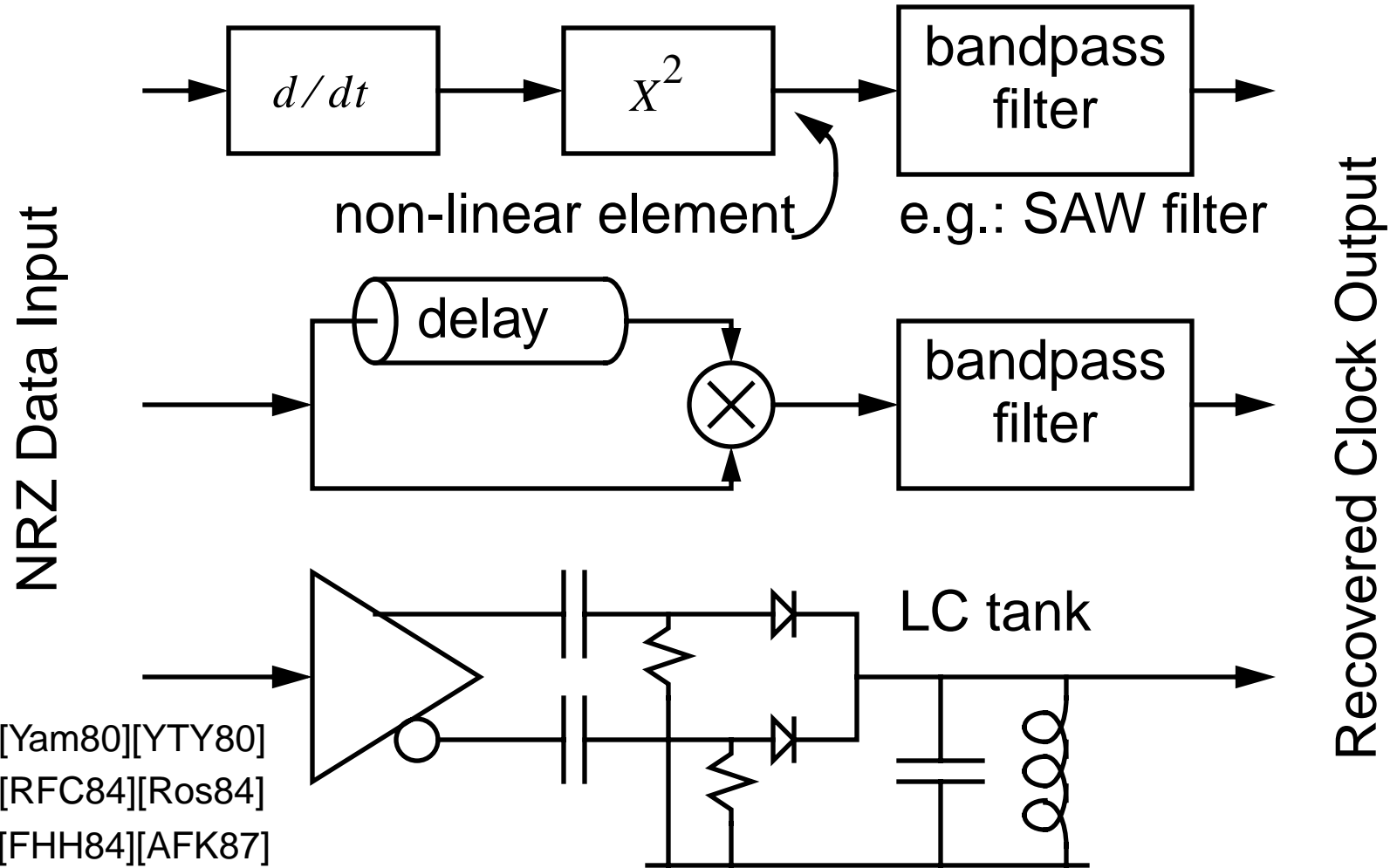


NRZ signalling is almost universally used.

Spectrum of NRZ data

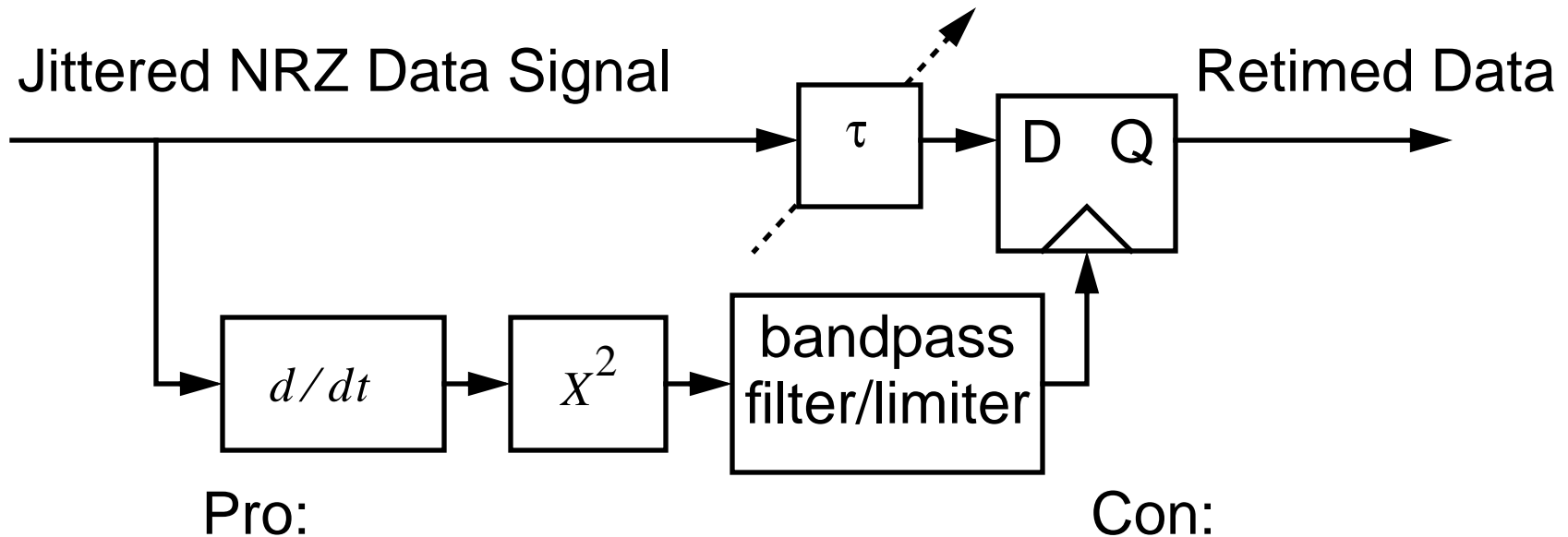


Filter Method Examples



(this last circuit can be thought of as an NRZ-RZ converter)

Summary of Filter Method



Very simple to implement

Can be built with microwave “tinkertoys” using coax to very high frequencies

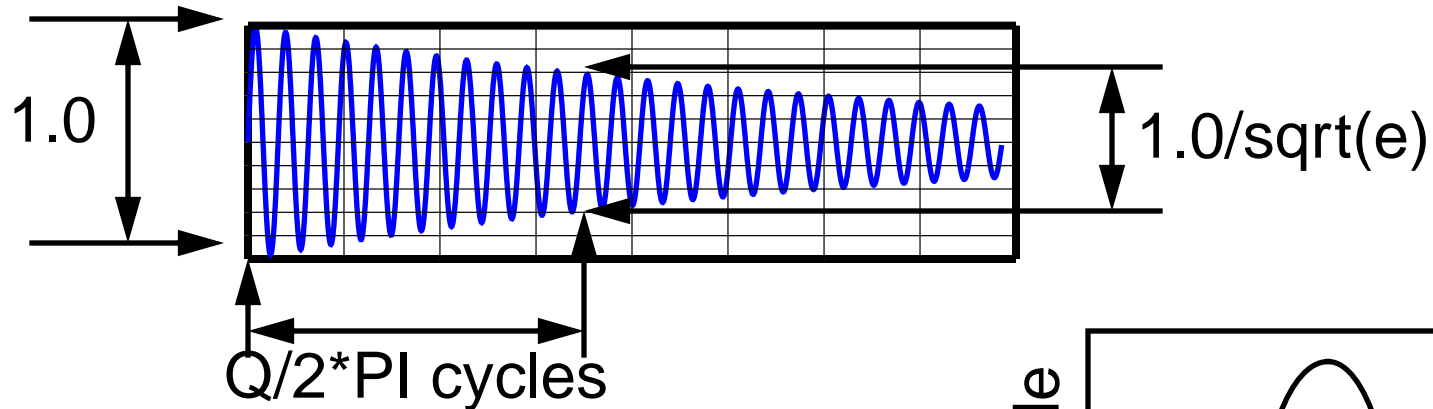
Temperature and frequency variation of filter group delay makes sampling time difficult to control

Narrow pulses imply high f_{τ}

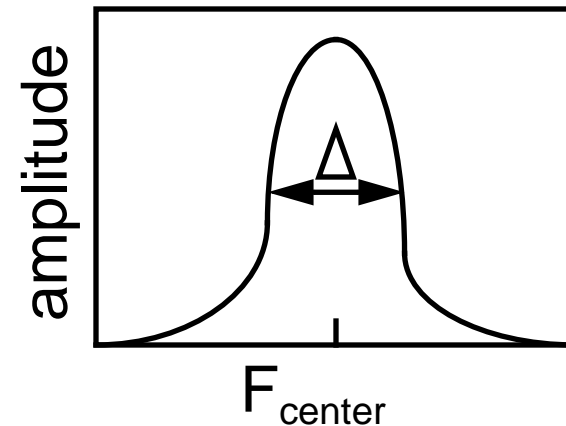
Hi-Q filter difficult to integrate

Q-Factor in resonant circuits

Voltage envelope of ringing circuit falls to $1/\sqrt{e}$ in Q radians.

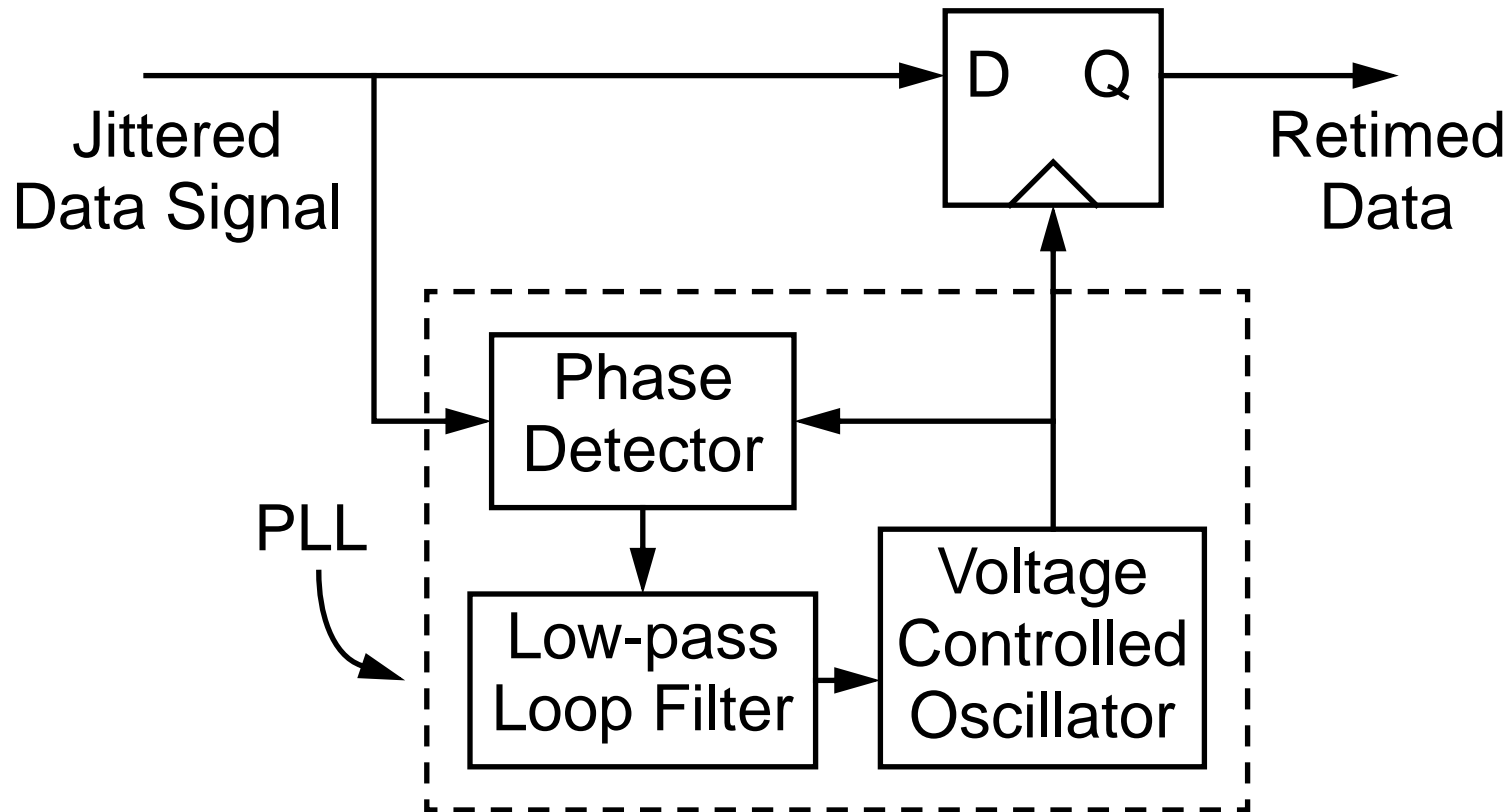


Q also equals the center frequency of a filter divided by the full-width of the resonance measured at the half power points:

$$F_{\text{center}} / \Delta$$


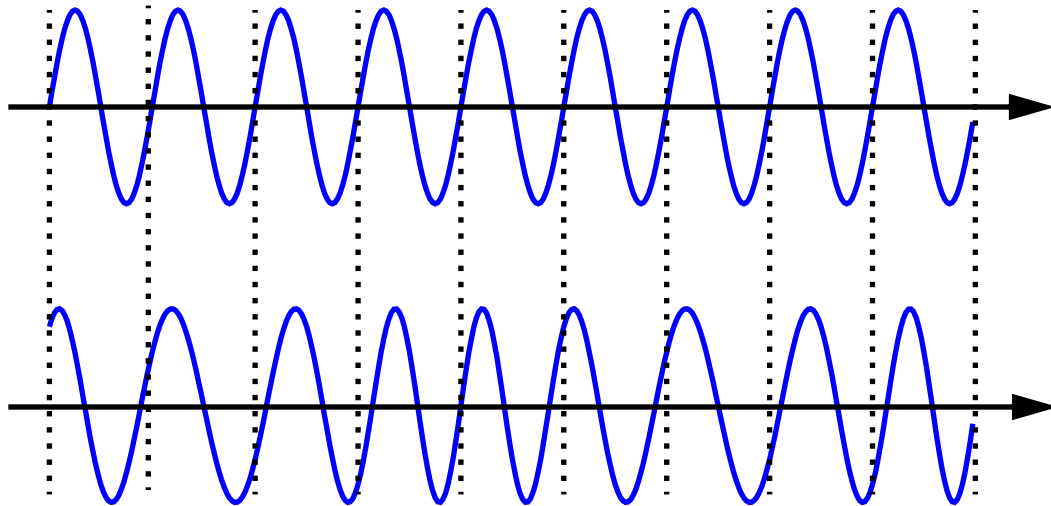
High-Q filter can be emulated by PLL with low loop B.W.

Data recovery with simple PLL



Everything in the simple PLL is easily integrable. The remaining problem is to match the recovered clock phase to the middle of the data eye. This can be difficult to achieve over all process variation at very high datarate/ft ratios.

Analytic Treatment of Jitter

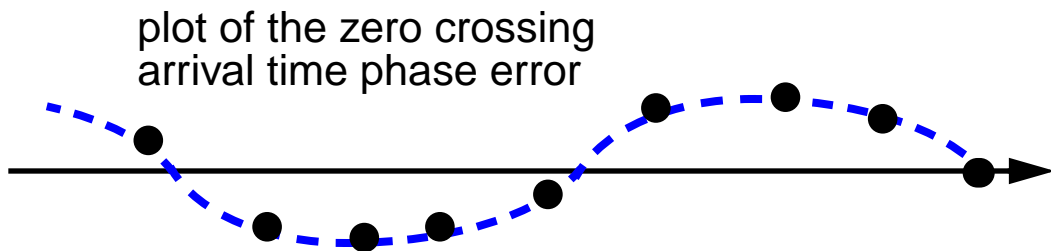


Perfect Clock:

$$x(t) = A \cos \omega_c t$$

Jittered Clock:

$$x(t) = A \cos [\omega_c t + \phi(t)]$$

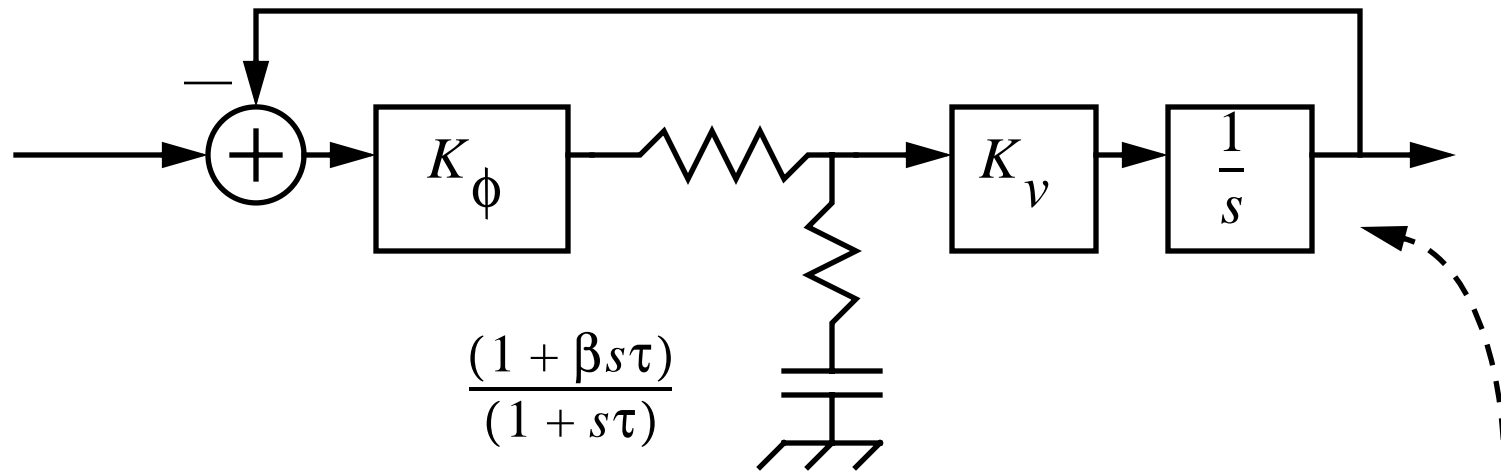
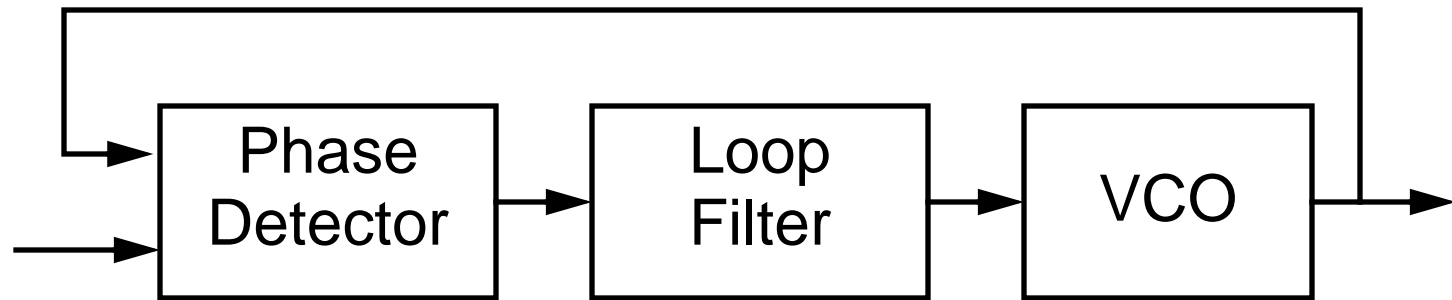


Jitter Signal:

$$x(t) = \phi(t)$$

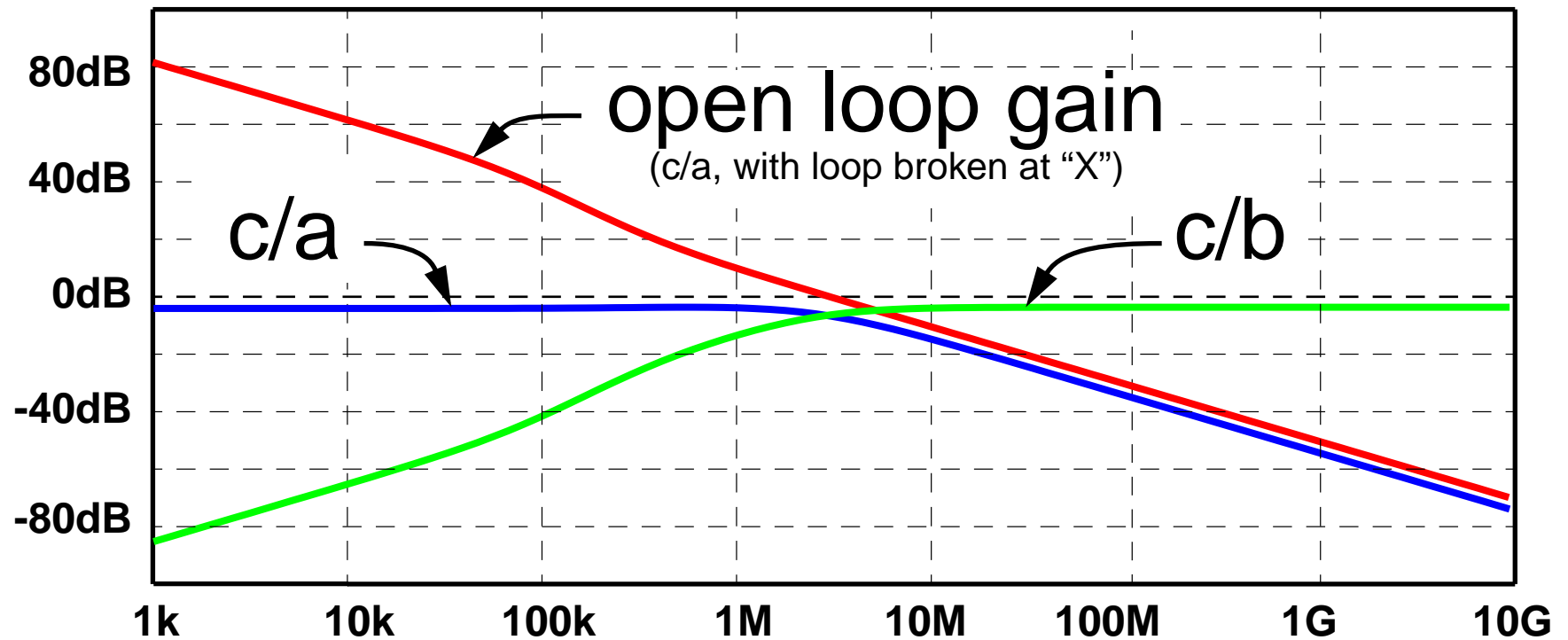
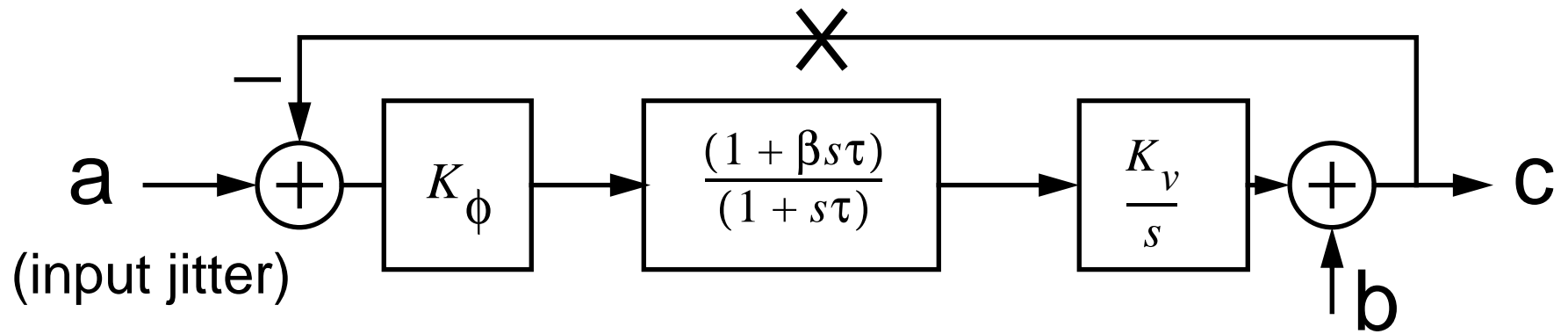
Practically, $\phi(t)$ is only measured at zero crossings, but is treated as a continuous time signal.

Model of linear phase-locked loop



Warning: Extra integration in VCO complicates the design!

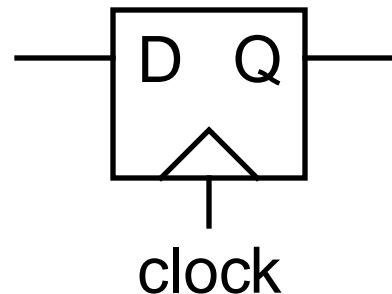
Linear loop frequency response



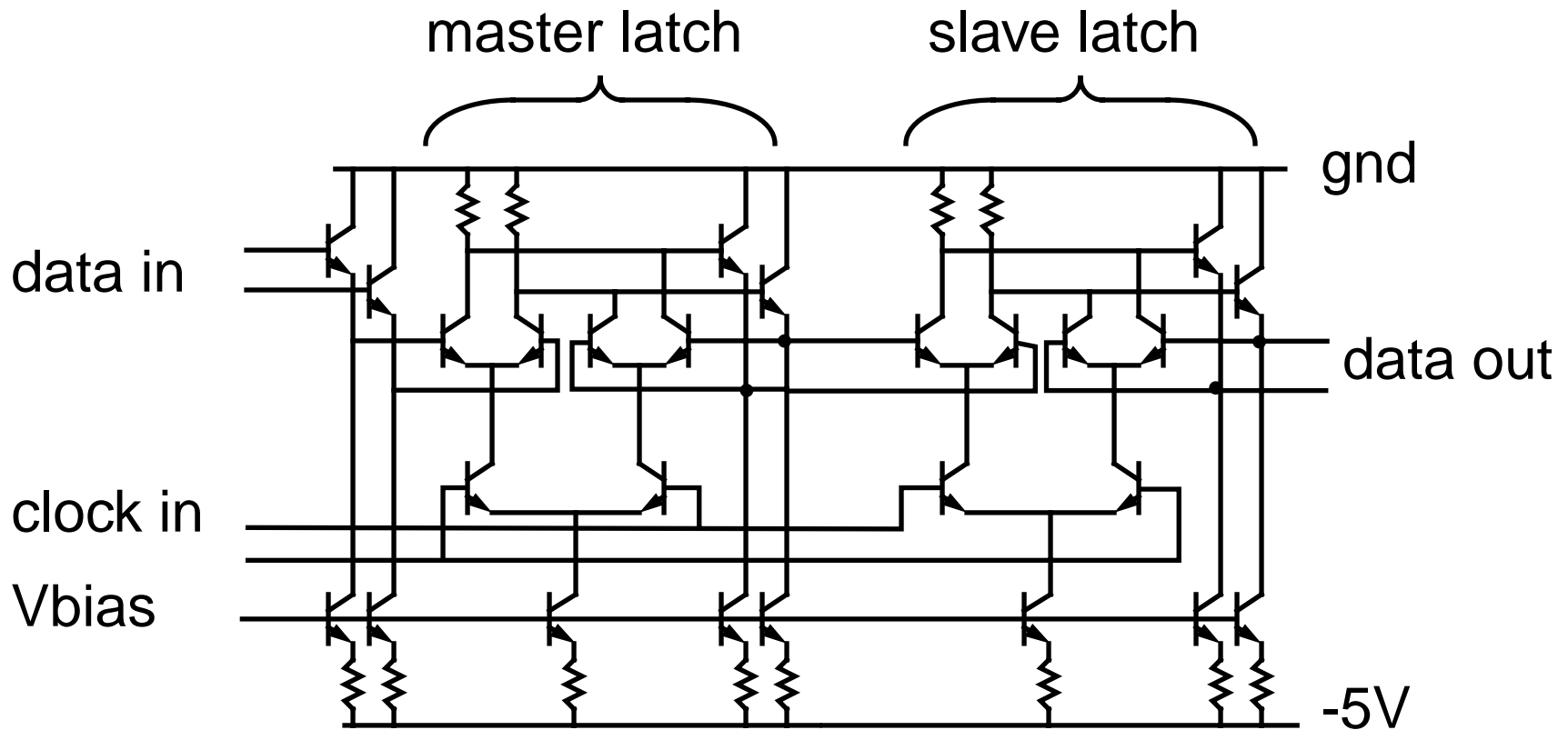
Decision Circuit

- Quantizes amplitude at precise sample instant and typically uses positive feedback to resolve small input signals
- A common choice in bipolar processes is a master/slave D-flip-flop carefully optimized for input sensitivity and clock phase margin
- To avoid hysteresis in CMOS processes, it is common to use a sense amp which is reset prior to each data sample

simplified
schematic
symbol:



Example Bipolar Decision Circuit



- many clever optimizations are possible

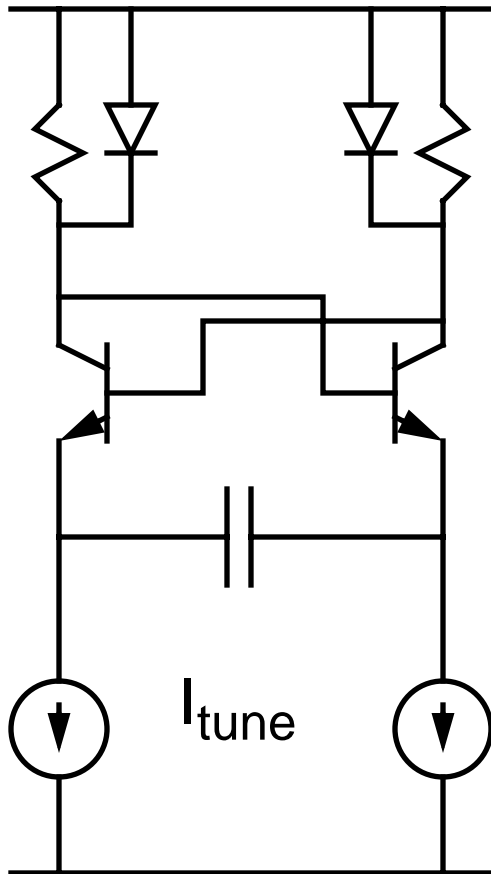
[OhT83][Con84][Lai90][Run91][Hau91]

VCO alternatives

	LC Oscillator	Multivibrator	Ring Oscillator
Speed	Technology Dependent 1-10's of GHz		
Phase Noise	Good	Poor	
Integration	Poor (L, Varactor)	Excellent	
Tunability	Narrow/Slow	Wide/Fast	
Stability	Good	Poor (needs acquisition aid)	
Other			Multi-Phase Clocks

- [Cor79, Ena87, Wal89, DeV91, Lam93, WKG94]

Multivibrator VCO



Capacitor is alternately charged and discharged by constant current

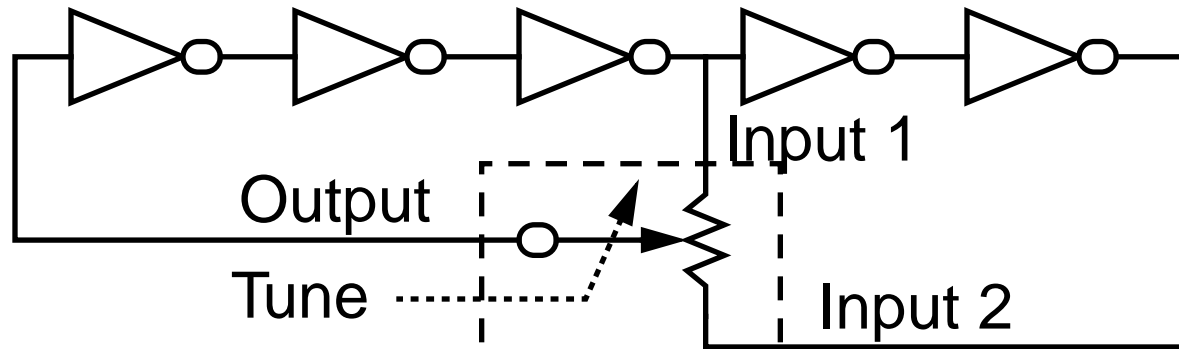
Tuned by varying I_{tune} in current source

Diode clamps keep output voltage constant independent of frequency

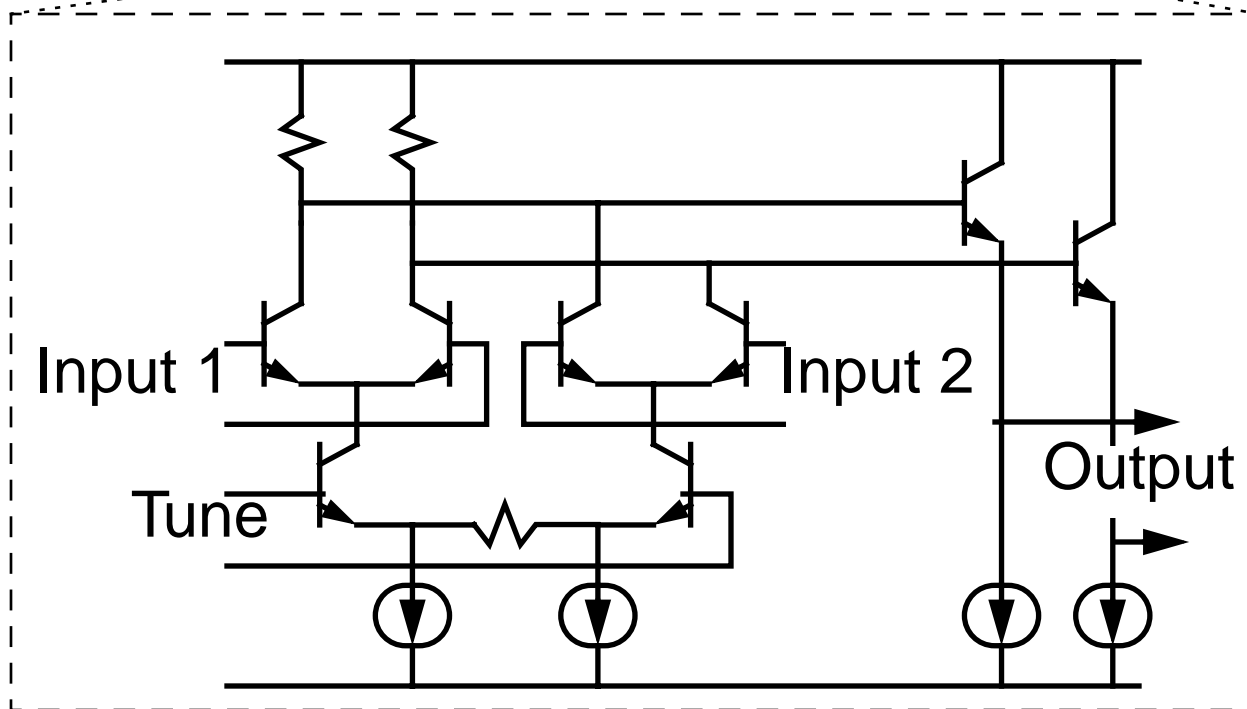
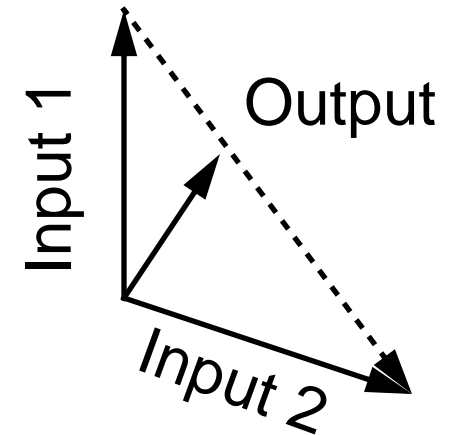
Relies on non-linear switching for oscillation behavior, and so is limited to moderate frequencies.

$$\text{Frequency} = \frac{I_{tune}}{4CV_{be}}$$

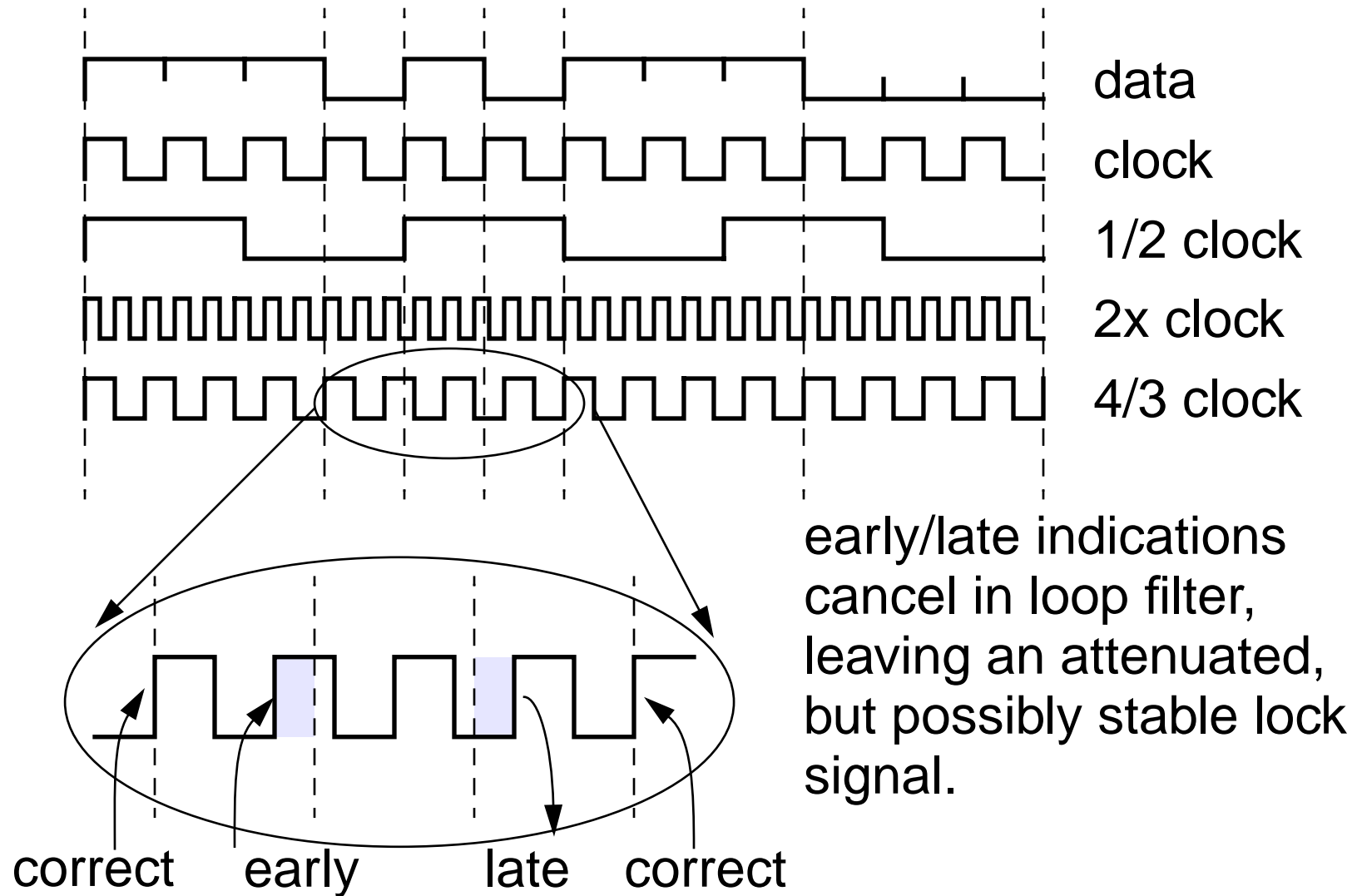
Example Ring Oscillator VCO



[SyA86]
[EnA87]
[Wal89]

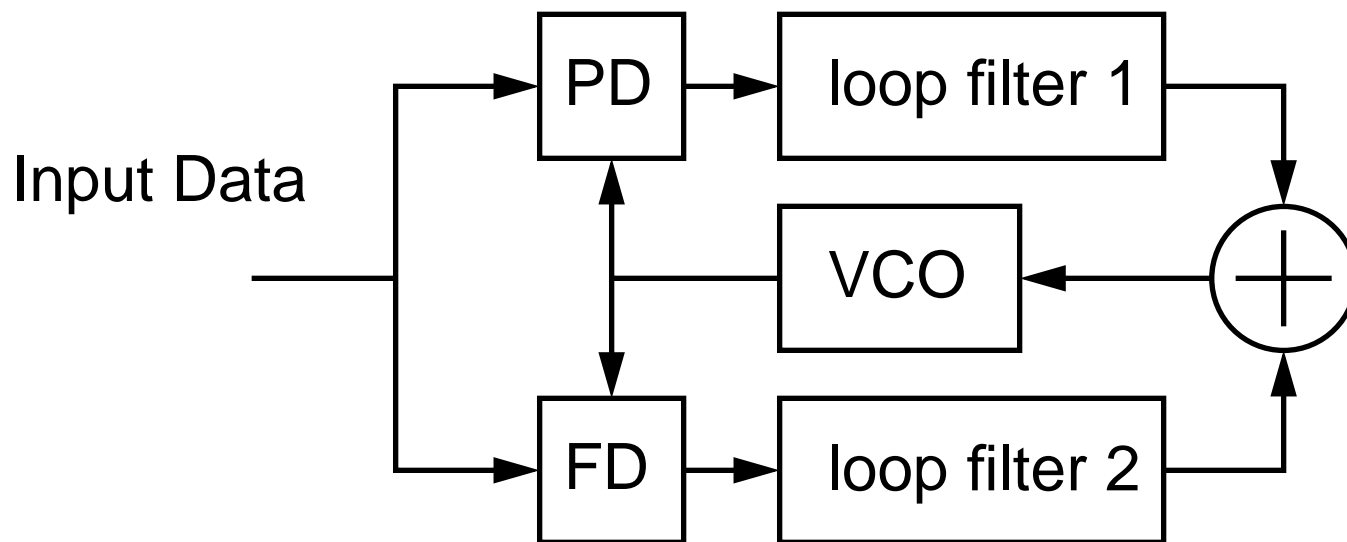


False or Harmonic Locking to Data



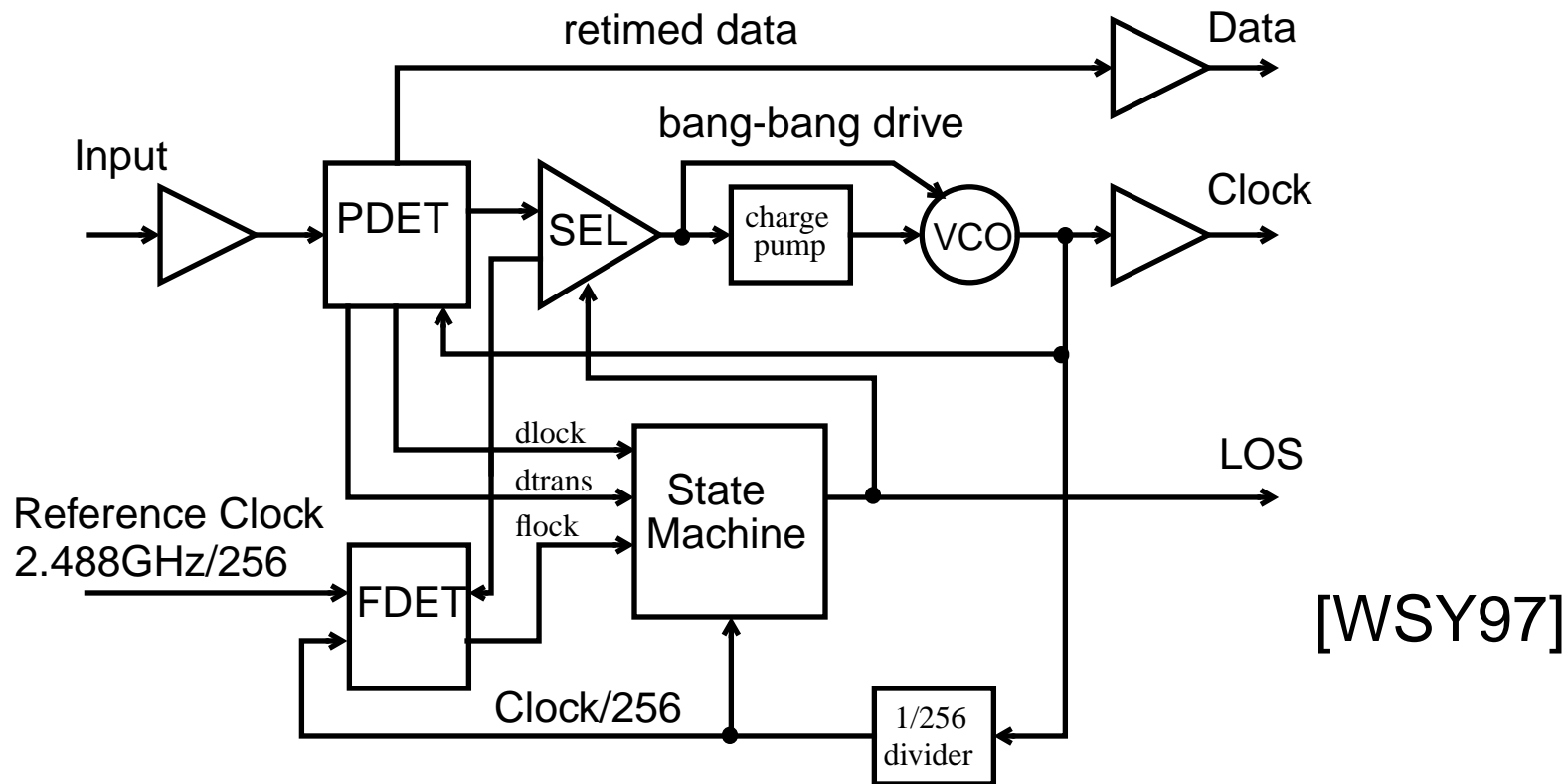
Aided Acquisition

- Tricky task due to Nyquist sampling constraints caused by stuttering data transitions



- Still subject to false lock if VCO range is too wide

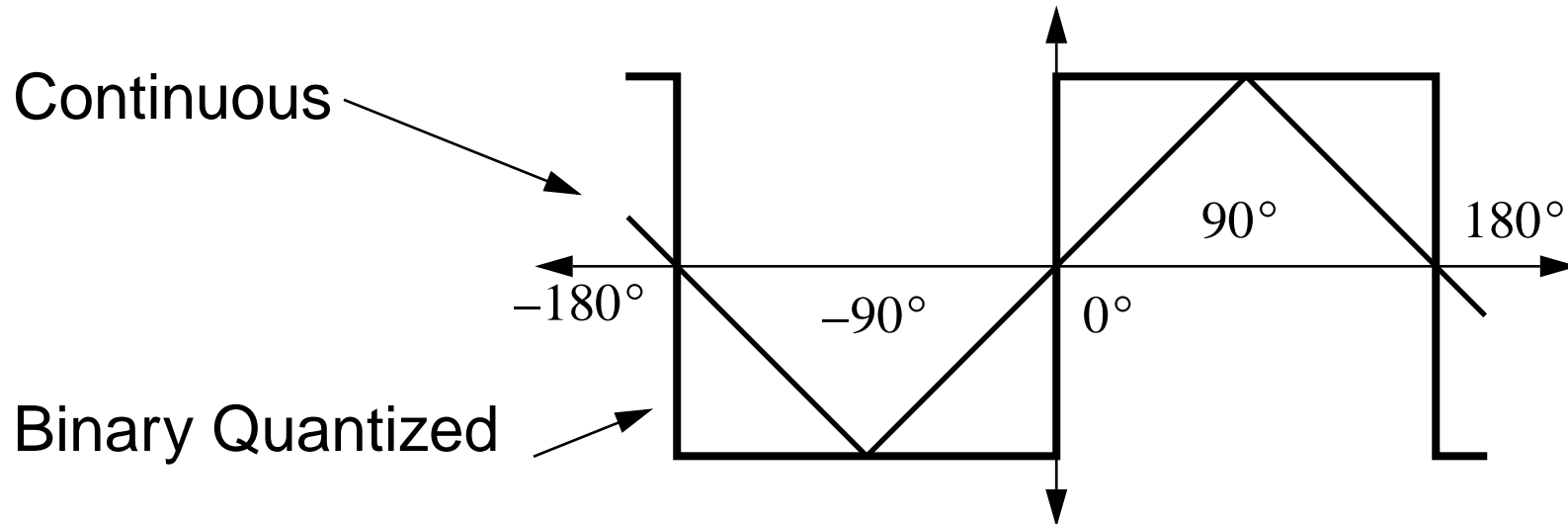
Training Loops



An increasingly common technique is to provide a reference clock to the CDR circuit. This allows the VCO process-variation to be dynamically trimmed out, avoiding false locking problems.

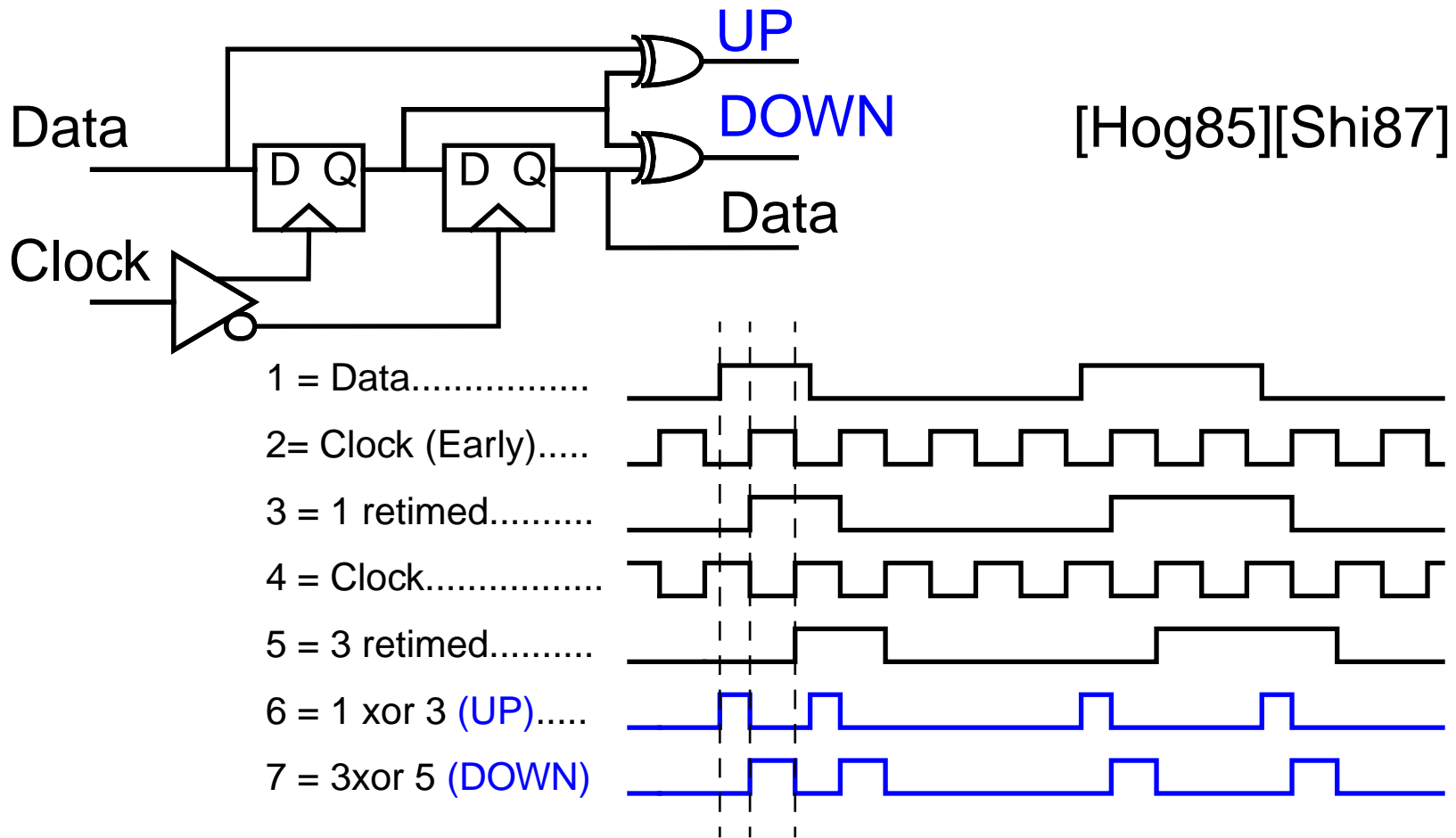
Phase Detectors

- Phase detectors generate a DC component proportional to deviation of the sampling point from center of bit-cell
- Phase detectors are:



- Binary quantized phase detectors are also called “Bang-bang”, or “early-late” phase detectors

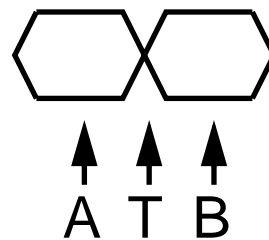
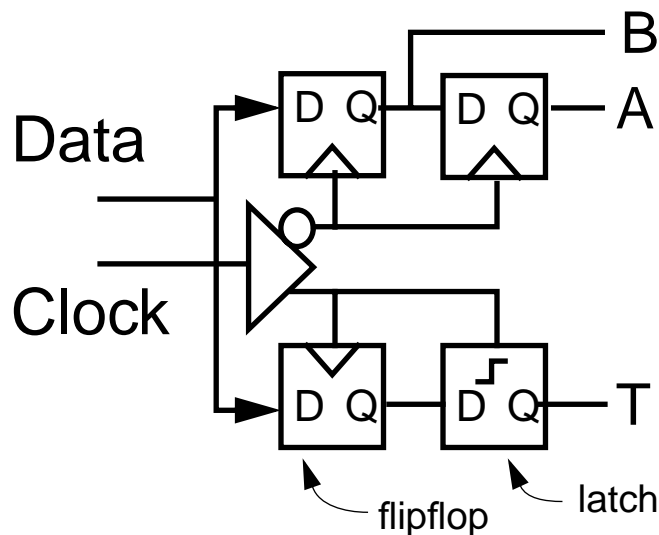
“Self-Correcting Phase Detector”



The “Hogge” detector is typical of linear phase detectors. It operates by creating pulses whose widths are equal to the phase error of the incoming data. These pulses may be difficult to produce at high speeds.

Early-Late Phase Detector

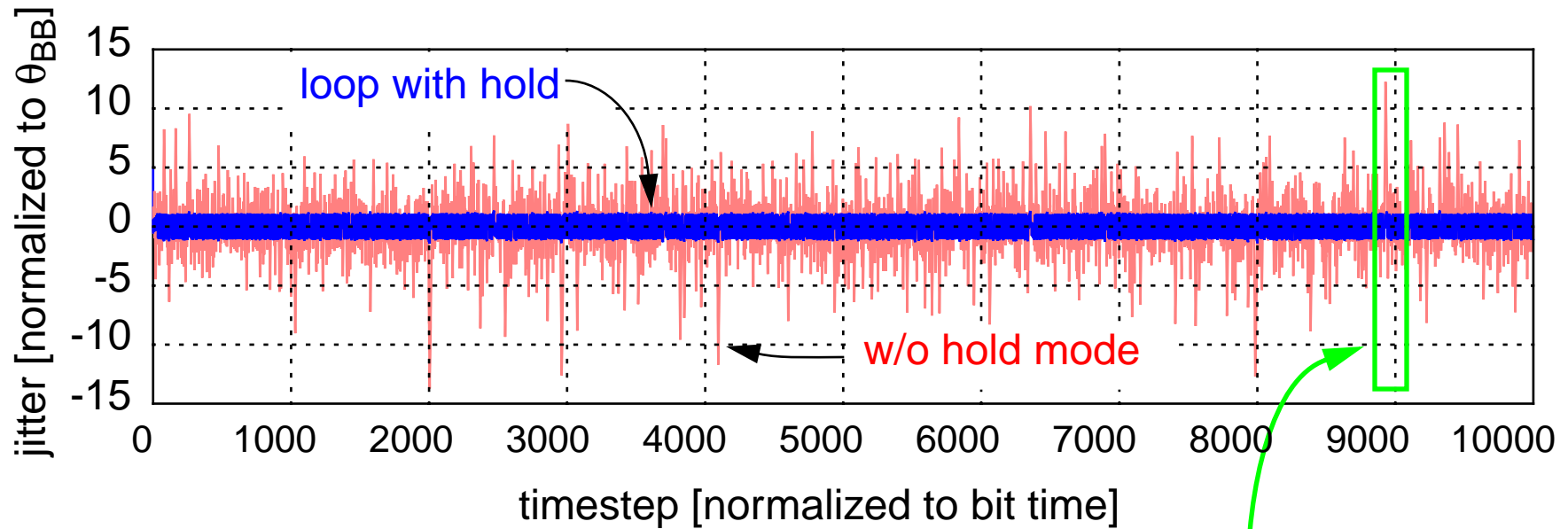
- NRZ data is sampled at each bit cell and near the transitions of each bit cell
- Transition sample polarity is compared with preceeding and following bits to deduce the phase error.
- Output is binary quantized, early-late phase indications, or ternary quantized if a hold-state is implemented.



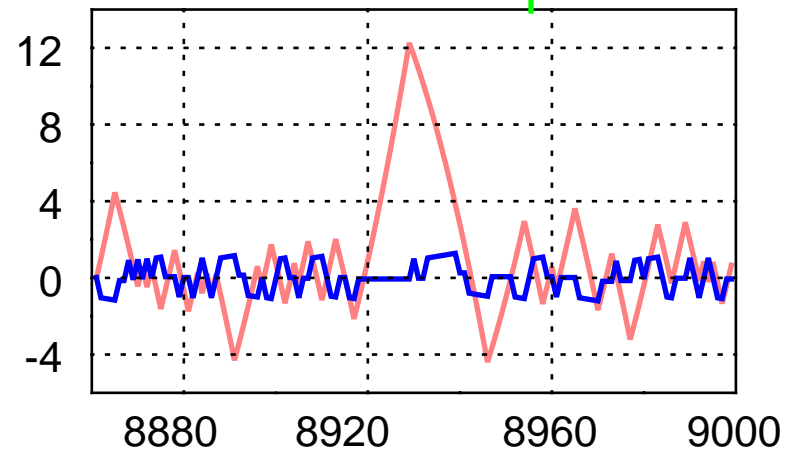
[Ale75][WHY91]
[LaW91][ReG73]

A	T	B	Output
0	0	0	hold
0	0	1	vco fast
0	1	0	?
0	1	1	vco slow
1	0	0	vco slow
1	0	1	?
1	1	0	vco fast
1	1	1	hold

BB/charge-pump w/wo hold state

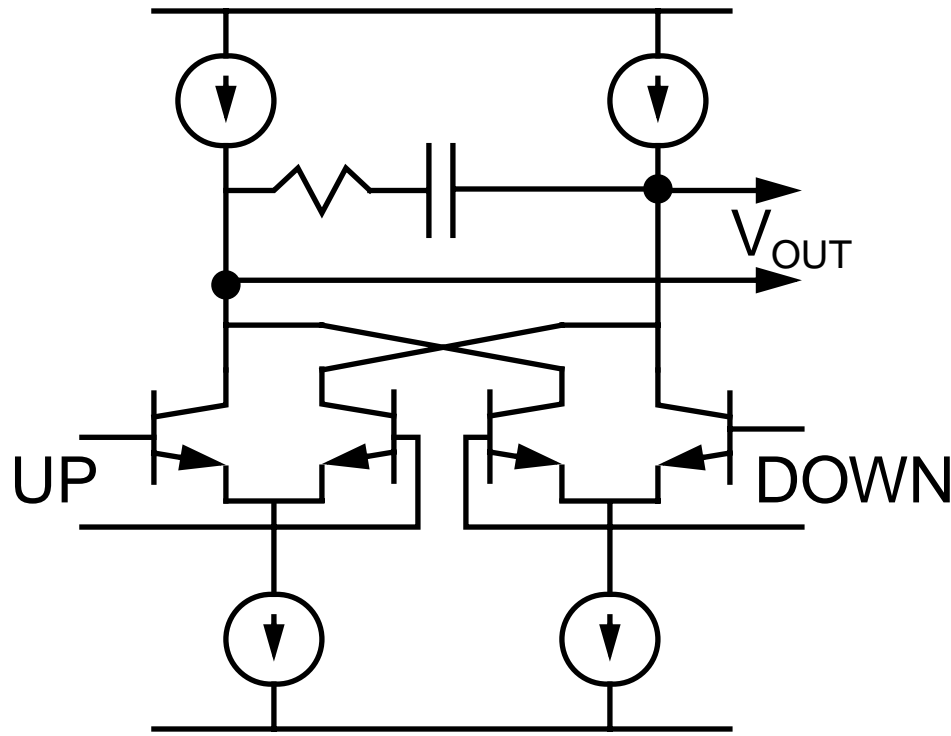


- hold-mode maintains VCO frequency when transitions are absent in the data.
- loop w/o hold has peak jitter *run-length* times worse than loop w/hold



(simulated with $\xi=100$, $p_{\text{transition}} = 50\%$)

Loop Filters



[Den88] [Dev91]
[LaW91] [WuW92]

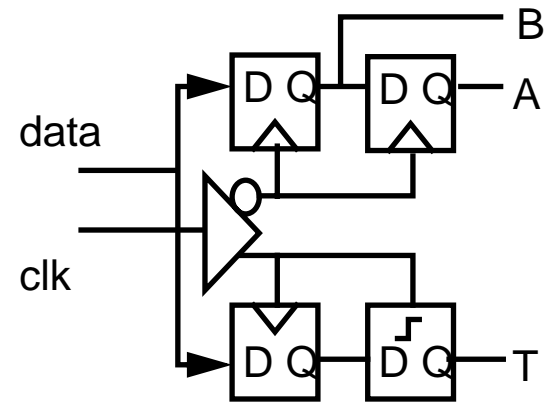
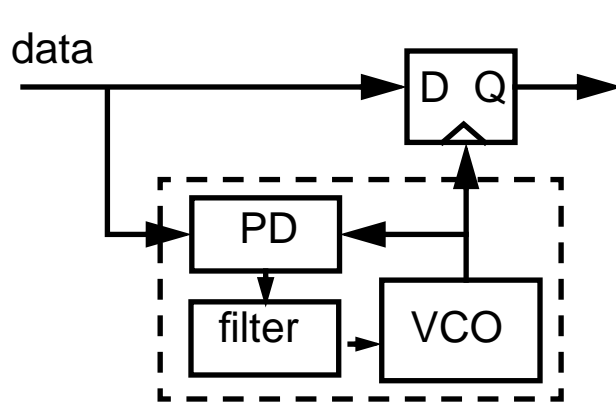
UP	DOWN	V_{OUT}
0	0	hold
0	1	ramp DOWN
1	0	ramp UP
1	1	hold

- should have provision for holding value constant under long run-length conditions
- may be analog (integrator) or digital (up-down counter) - but *watch out for metastability!*

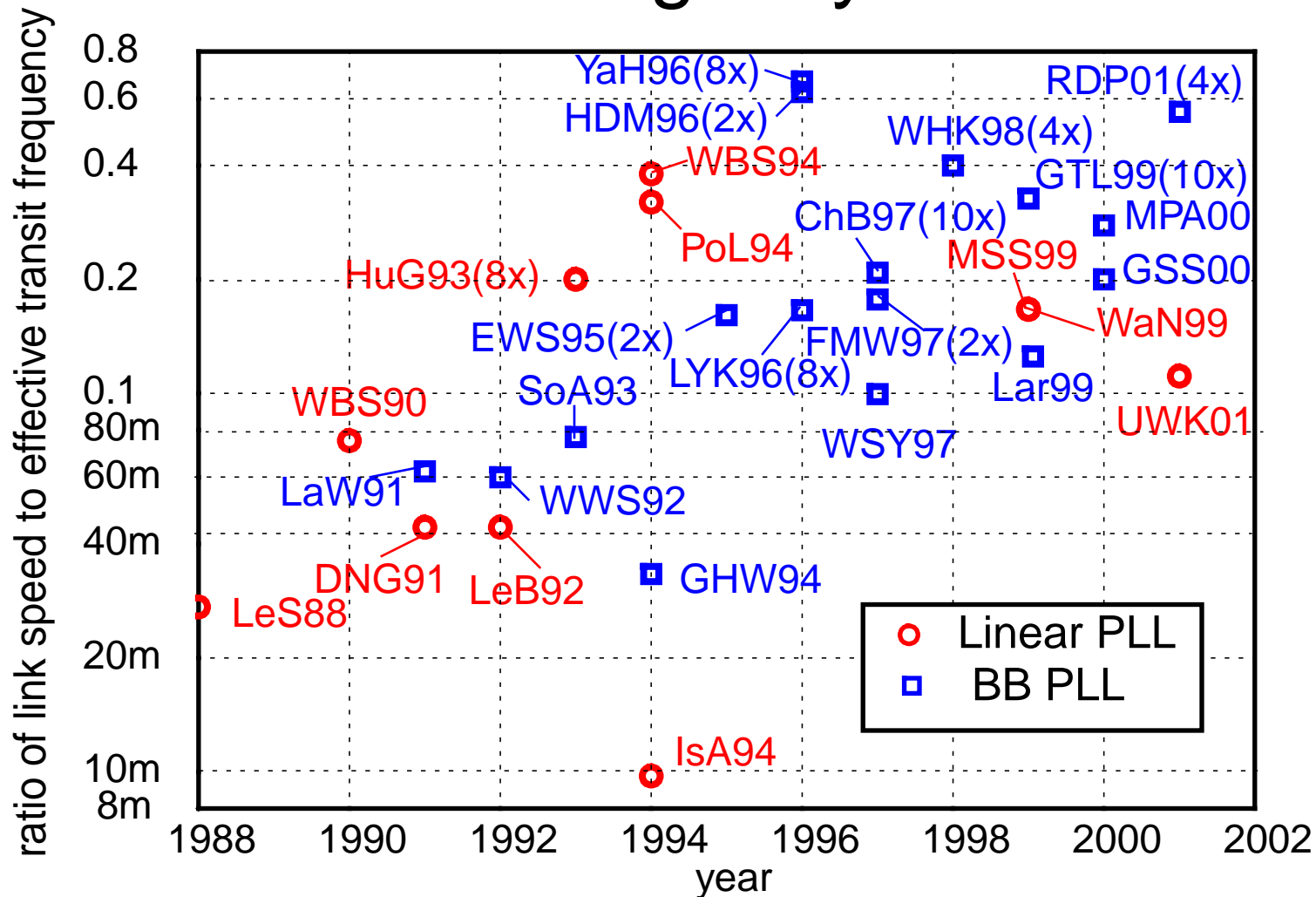
Bang-bang PLL Theory

Why bother with a BB loop?

- it may be difficult to maintain optimum sampling point with traditional PD/PLL or with filter method over process, temperature and supply variation
- Narrow pulses of linear PD's may not work well at extremely high bit rates
- for monolithic implementation, BB PD has excellent match between retiming latch and PD latch - allows for operation at highest latch toggle frequency

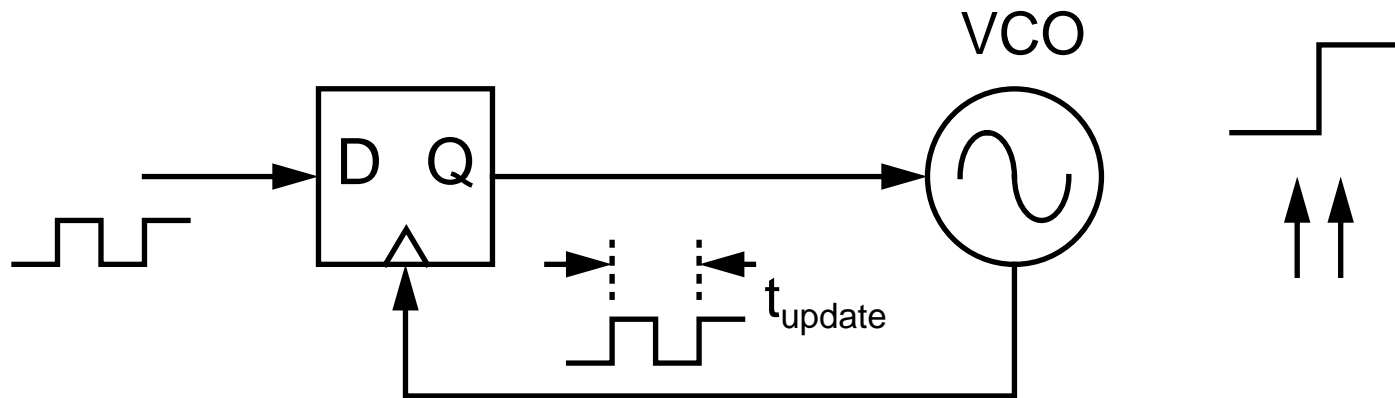


CDR PLL design style over time



BB PLLs have the advantage of precise sample point alignment based on layout symmetry. This makes BB PLLs predominate as designs push data rate towards the process transit frequency limit. (number of retiming phases shown in ()).

Simple First Order BB loop

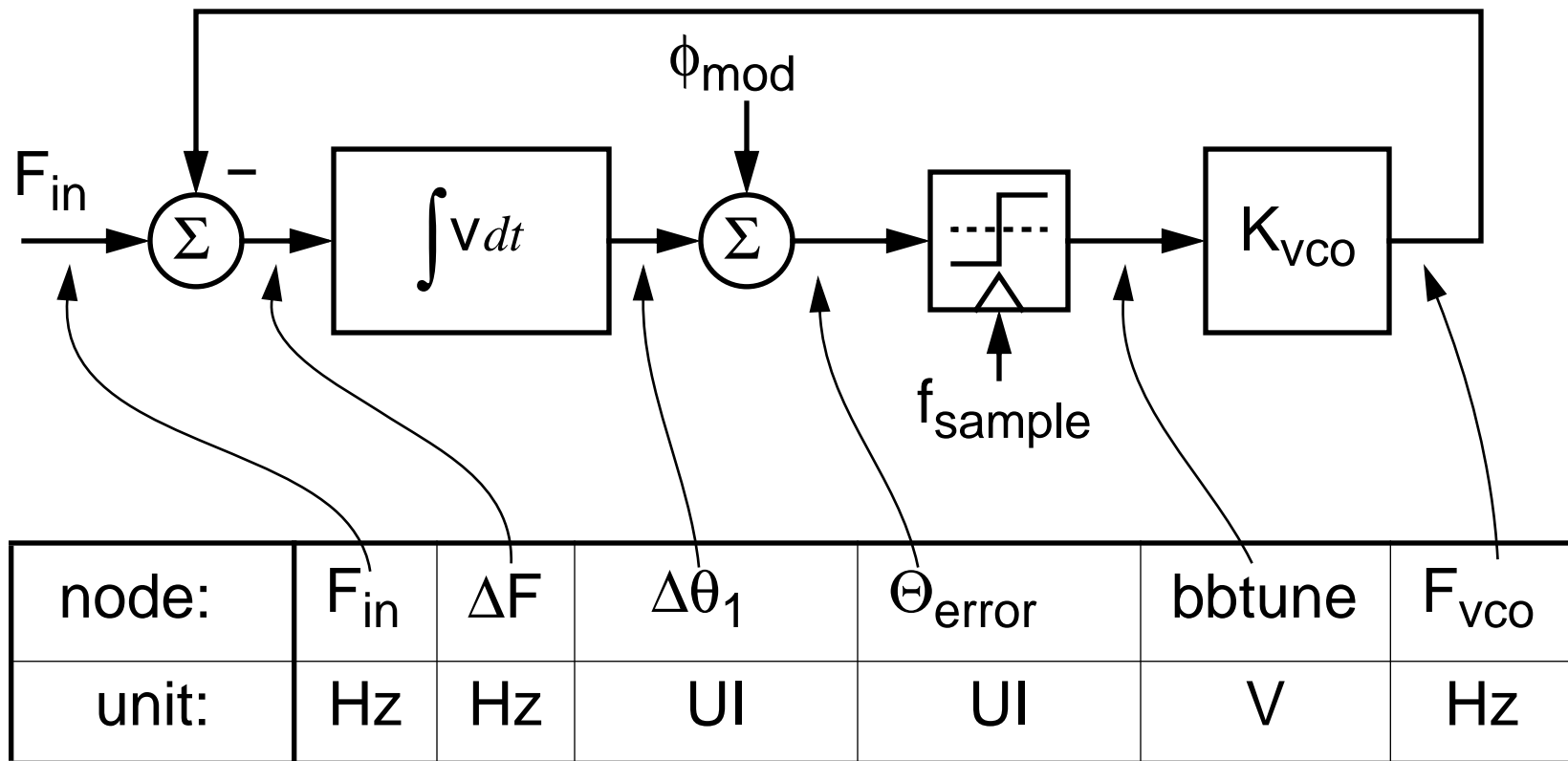


- VCO runs at two discrete frequencies: $f_{nom} \pm f_{bb}$.
- Phase error is evaluated at a discrete time interval t_{update} . In general, this can be approximated by the mean transition time of the data.
- A simple D-flip-flop serves as a bb-phase detector if locking to a clock rather than to a data signal.

Efficient Simulation Strategy

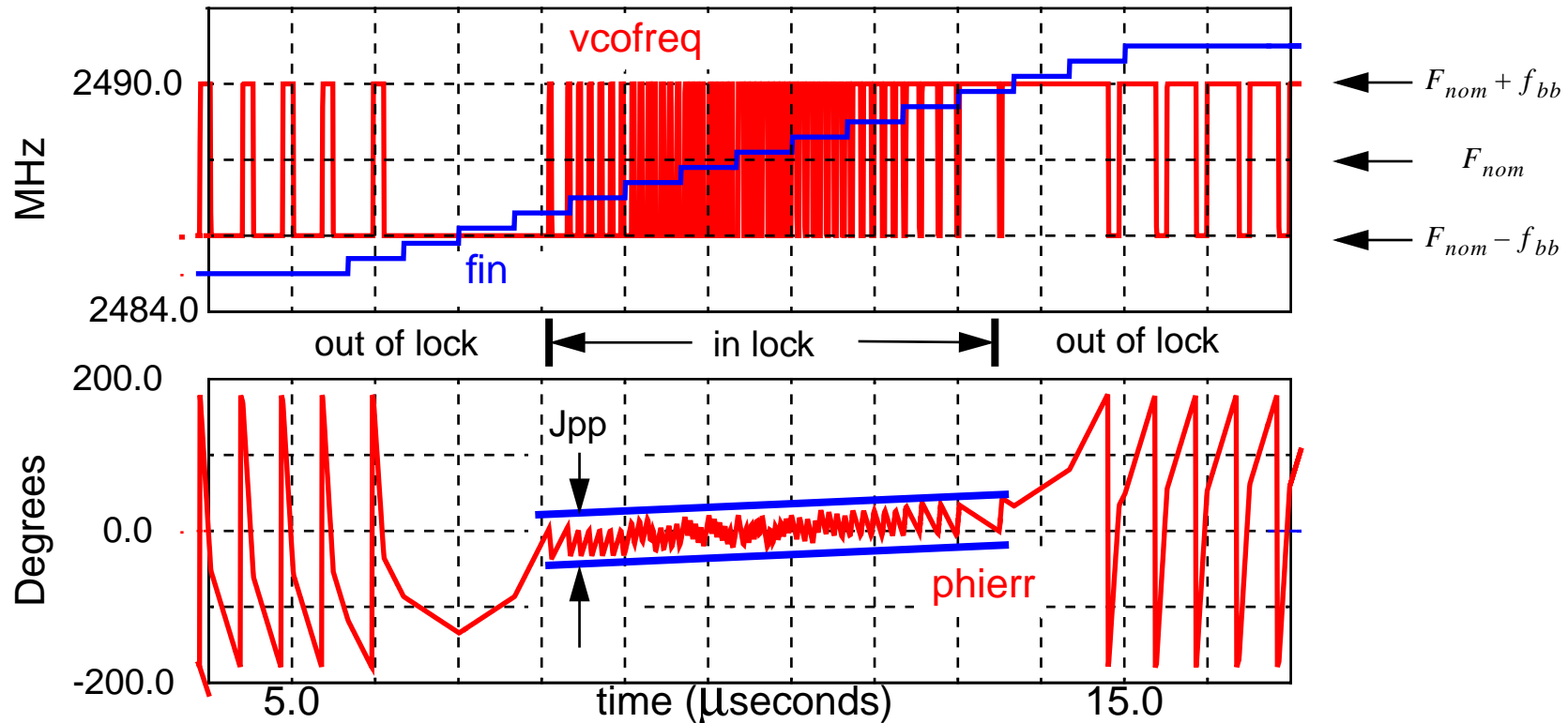
- Simulating the *VCO waveform* is unnecessary to accurately model ideal PLL behavior.
- Only frequency and phase is needed.
- Model all circuit time-varying state variables as voltages.
- Convert between frequency and phase variables with explicit integration block.

Model of First-order Loop



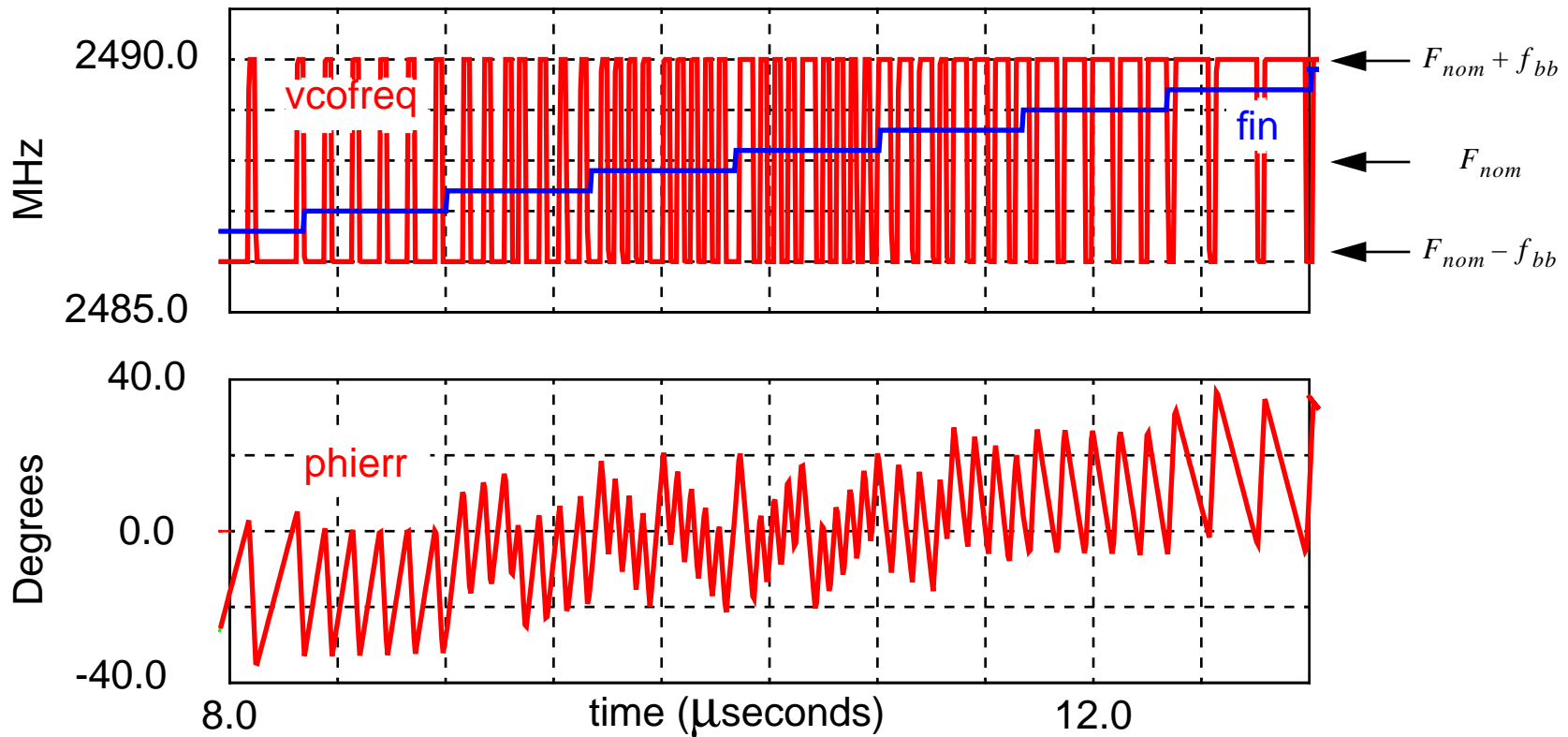
The tricky bit is to define the loop in terms of an input frequency rather than an input phase by pulling the VCO integral through the input summation. This allows easy simulation of both frequency and phase steps.

Lock Range for 1st-order loop



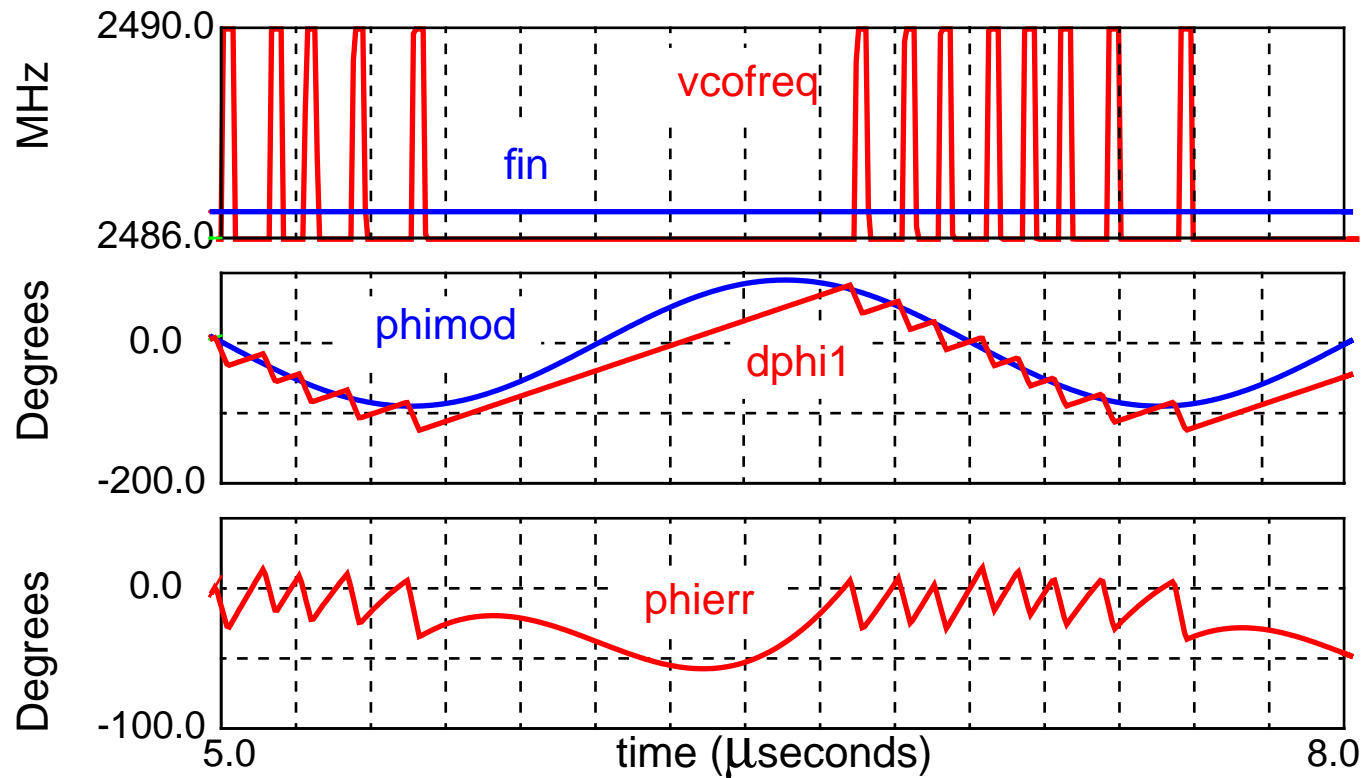
The loop is “locked” whenever the input frequency is bracketed by the two VCO frequencies. The rapid alternation between frequencies slightly too high and slightly too low create a hunting jitter (J_{pp}).

1st-order loop: locked region



The phase detector duty-cycle is proportional to the average frequency error.

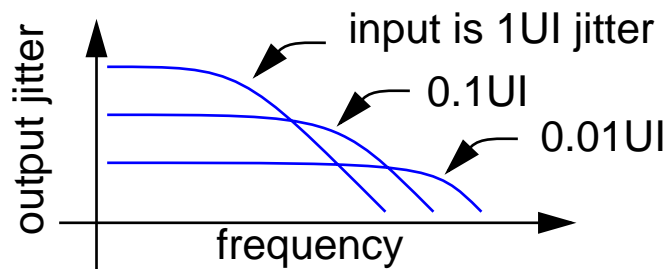
1st-order loop: slew-rate limiting



Although the average input frequency (f_{in}) lies within the lock range of the loop, the added sinusoidal jitter ($phimod$) causes the instantaneous input frequency to exceed the VCO range. The loop phase ($dphi1$) stops toggling and goes into slew rate limiting, leading to a phase error ($phierr$).

Summary of 1st-order loop

- Lock range: $(f_{nom} - f_{bb}) < f_c < (f_{nom} + f_{bb})$.
- Jitter (pk/pk in UI): $J_{pp} = 2 \cdot t_{update} \cdot f_{bb}$.
- Bang-bang loop tracking is slew-rate limited. The effective loop bandwidth is amplitude dependent.



- The maximum amplitude of phase modulation at frequency f_{mod} before onset of slew-rate limiting:
 $A_{UI} = f_{bb} / f_{mod}$.

Summary of 1st-order loop, cont.

- If locked, then the duty cycle C , must result in the average loop frequency being equal to the input frequency f_c ,

$$f_c = f_{nom} + \Delta f = C(f_{nom} + f_{bb}) + (1 - C)(f_{nom} - f_{bb})$$

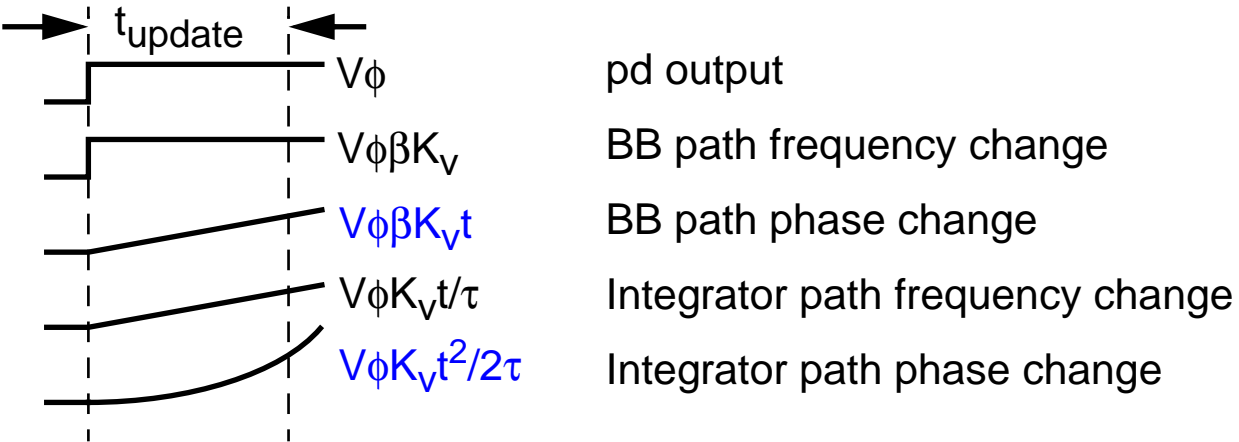
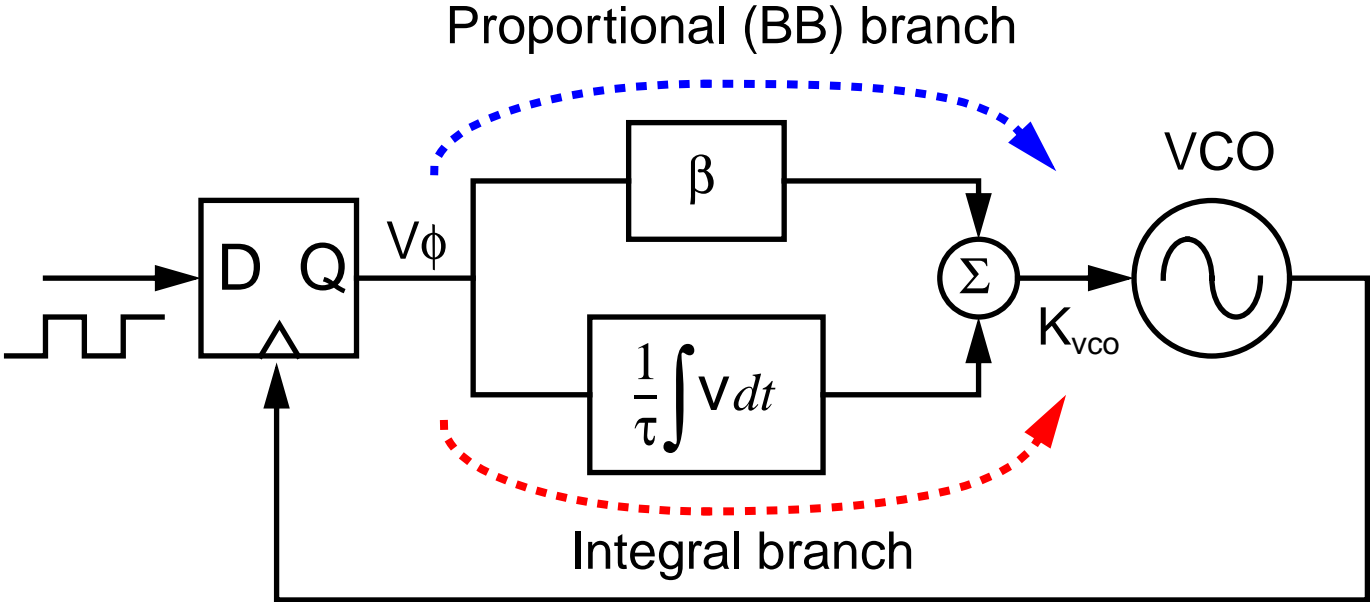
- Phase detector average duty cycle C , given by

$$\left(\frac{1}{2} + \frac{\Delta f}{(2 \cdot f_{bb})} \right) \quad (\text{proportional to } \Delta f \text{).}$$

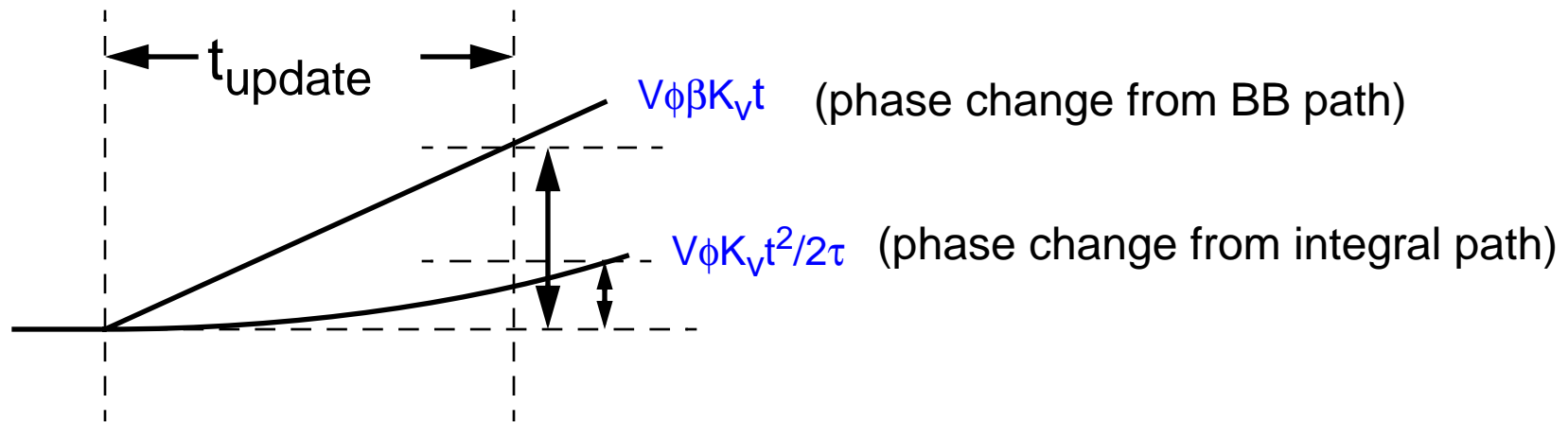
Observations

- Jitter generation, Jitter transfer bandwidth, Jitter tolerance and frequency lock range are all inconveniently controlled by one parameter, f_{bb} .
- Phase detector average duty-cycle is proportional to frequency error.
- Strategy: Use the average duty cycle to control loop center frequency. This decouples the lock range from jitter tolerance/generation giving more design freedom.
- If the center frequency control loop is slow enough, the resulting loop behavior will be very similar to a simple first order loop, but with extended frequency lock capability.

2nd-order BB loop



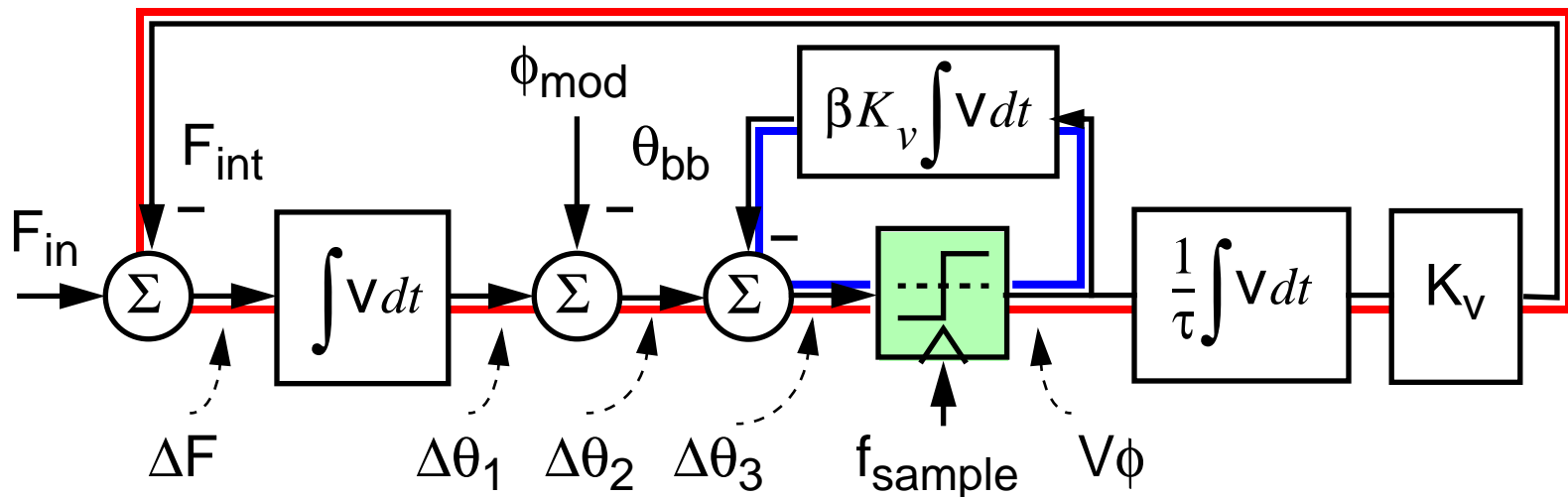
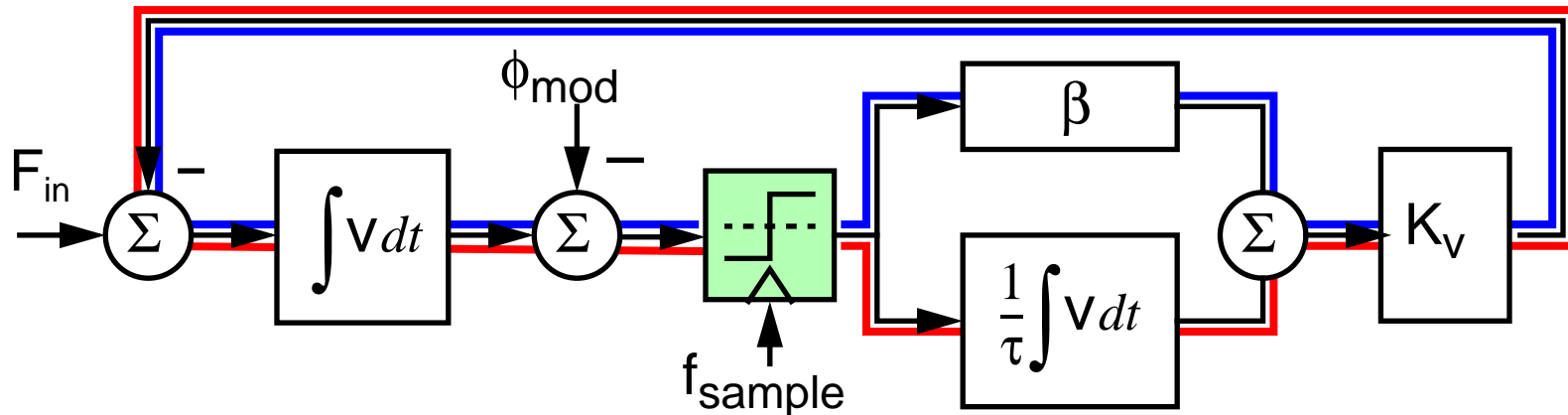
Stability Factor ξ



To quantify the relative independence of the two feedback loops, take ratio of phase change from BB path to the phase change of the integral path:

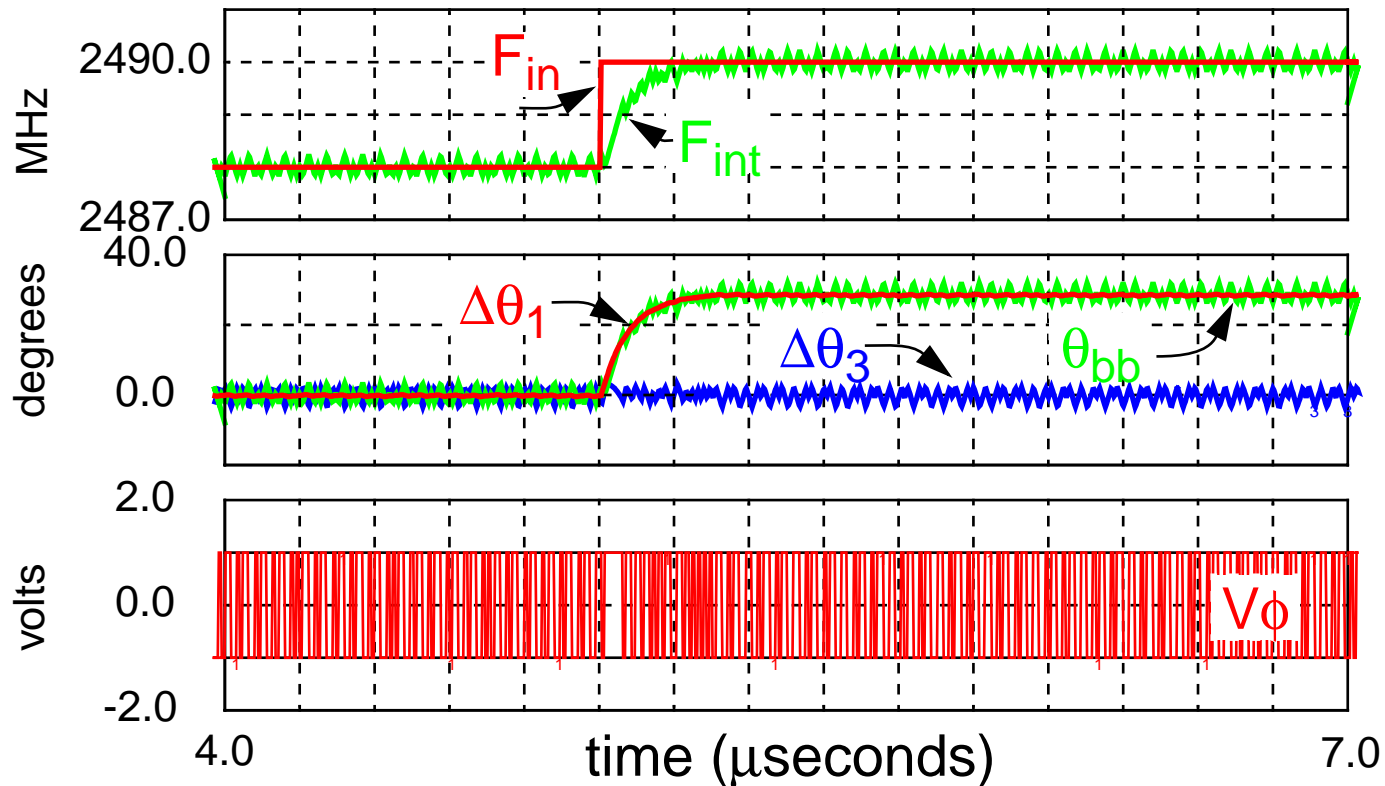
$$\xi \equiv \frac{\Delta\theta_{bb}}{\Delta\theta_{int}} = \frac{\beta V_\phi K_v t}{V_\phi K_v t^2 / (2\tau)} \Big|_{t = t_{update}} = \frac{2\beta\tau}{t_{update}}$$

redrawing the 2nd-order loop



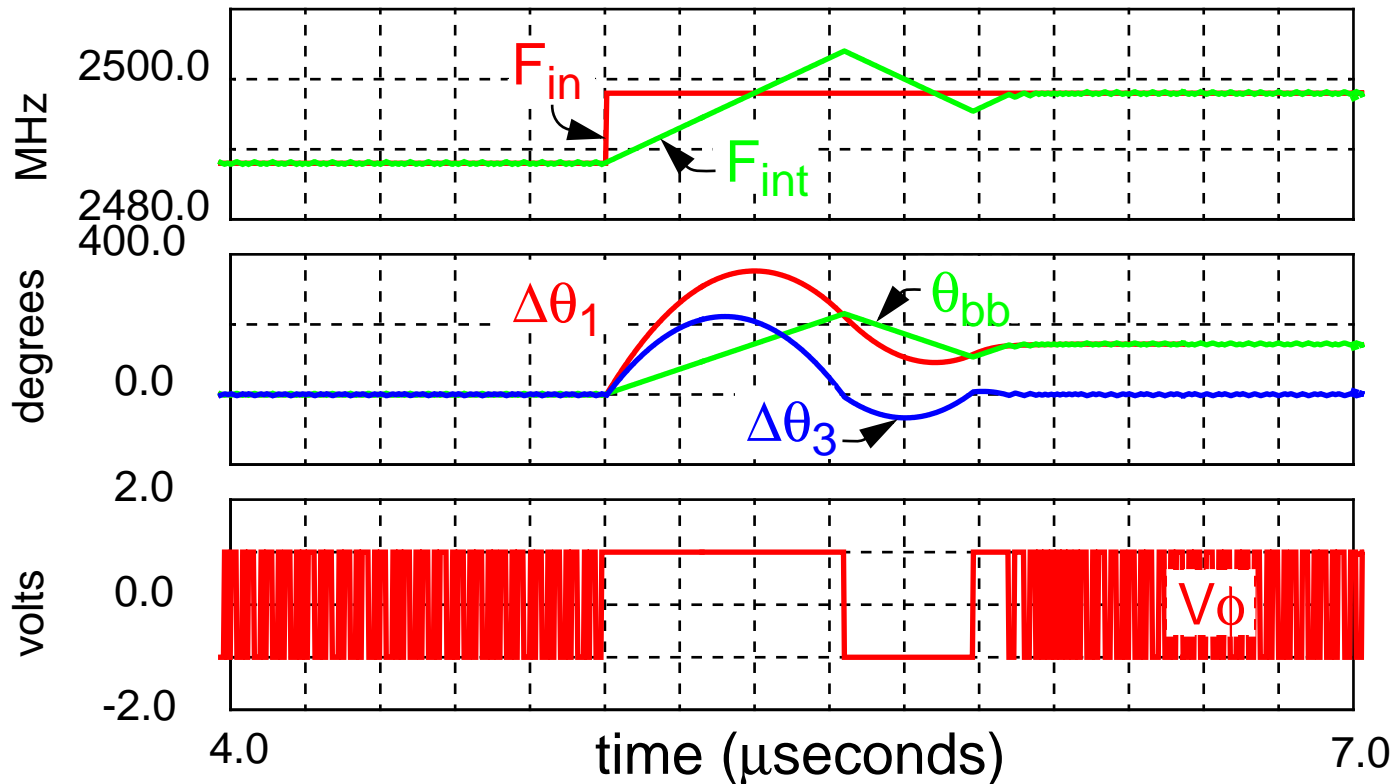
Noticing that $V\phi$ is proportional to ΔF , the system can be transformed into an inner first order bb-loop PLL (in blue) surrounded by an outer low-bandwidth frequency tracking loop (in red).

2nd-order loop: small step in F



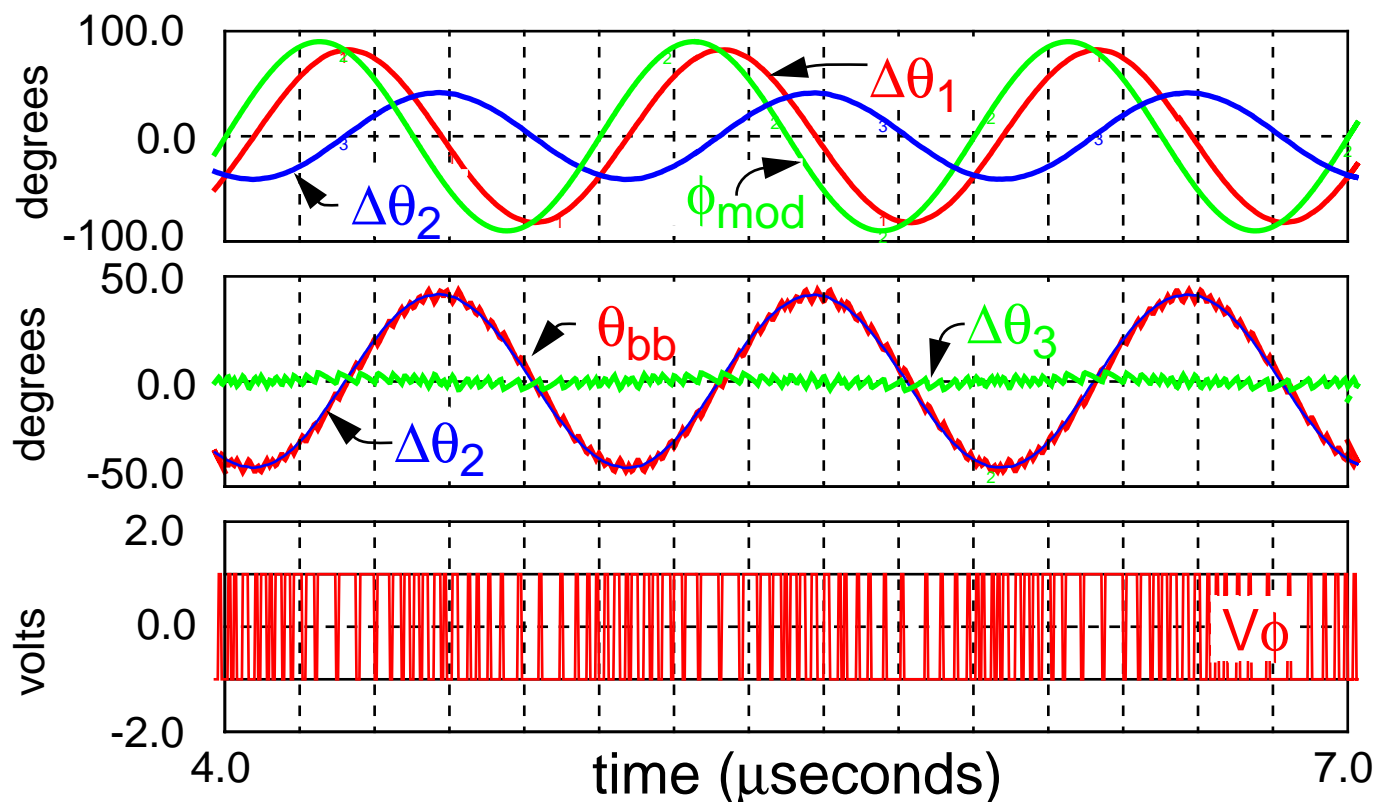
A step change in input frequency F_{in} produces a slow response F_{int} in the outer, integral loop. The resulting phase error $\Delta\theta_1$ is tracked by the inner bang-bang loop θ_{bb} to produce the final sampler phase error $\Delta\theta_3$. Notice that, unlike a linear PLL, there is no jitter accumulation at the sampler.

2nd-order loop: large step in F



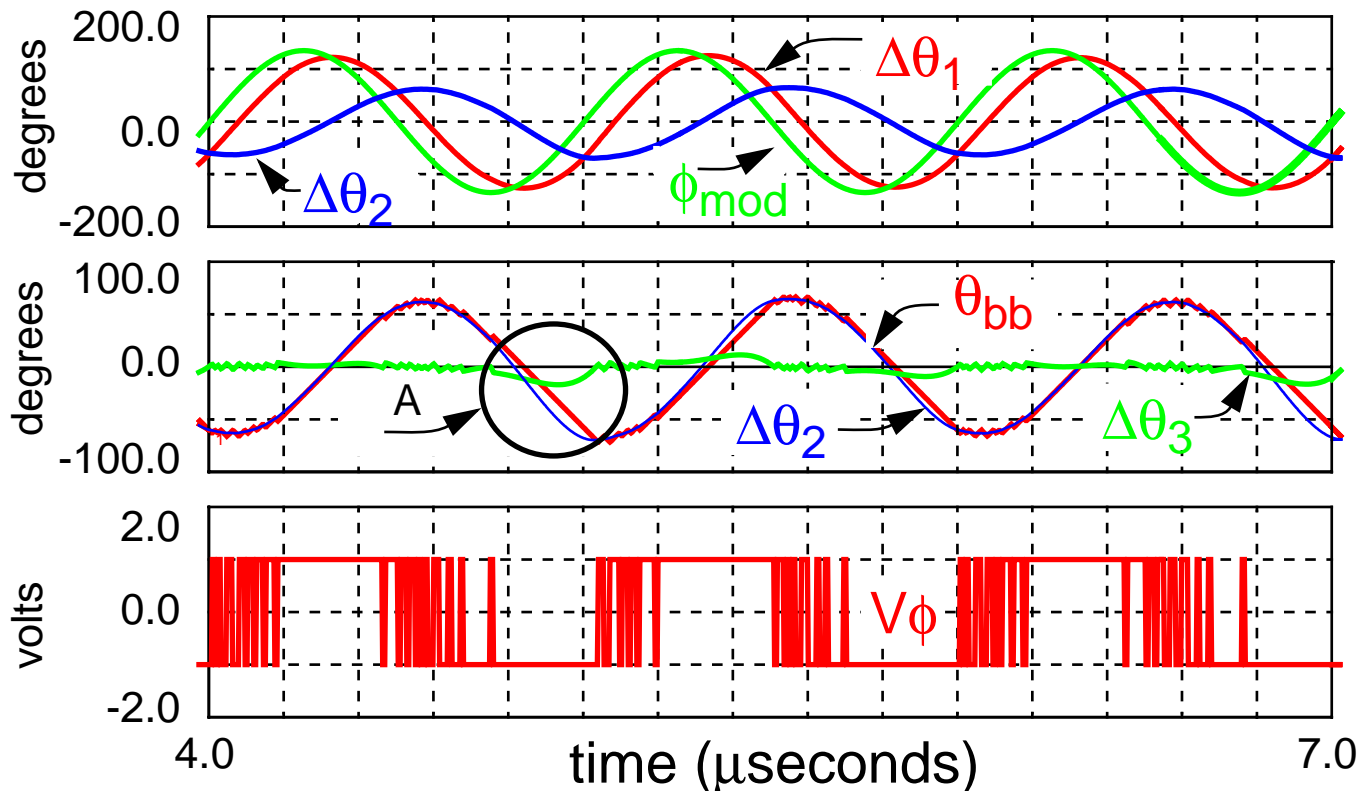
In this simulation, the input frequency step is bigger than f_{bb} , so the loop goes into slew rate limiting, leading to a transient phase error $\Delta\theta_3$ at the sampler. A fancier loop could detect slew rate limiting by the lack of PD transitions, and adaptively increase the loop frequency step size.

2nd-order loop: phase jitter tracking



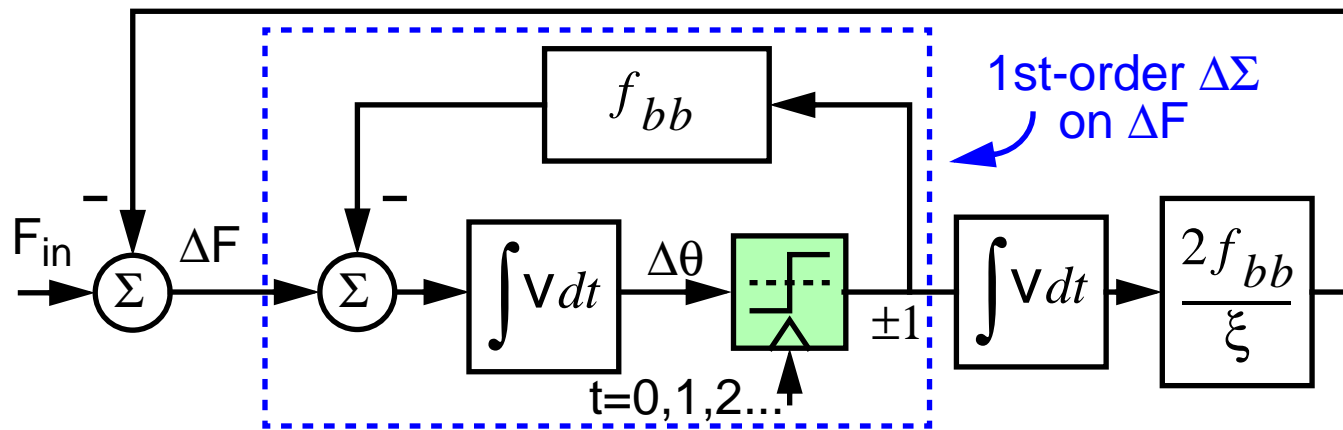
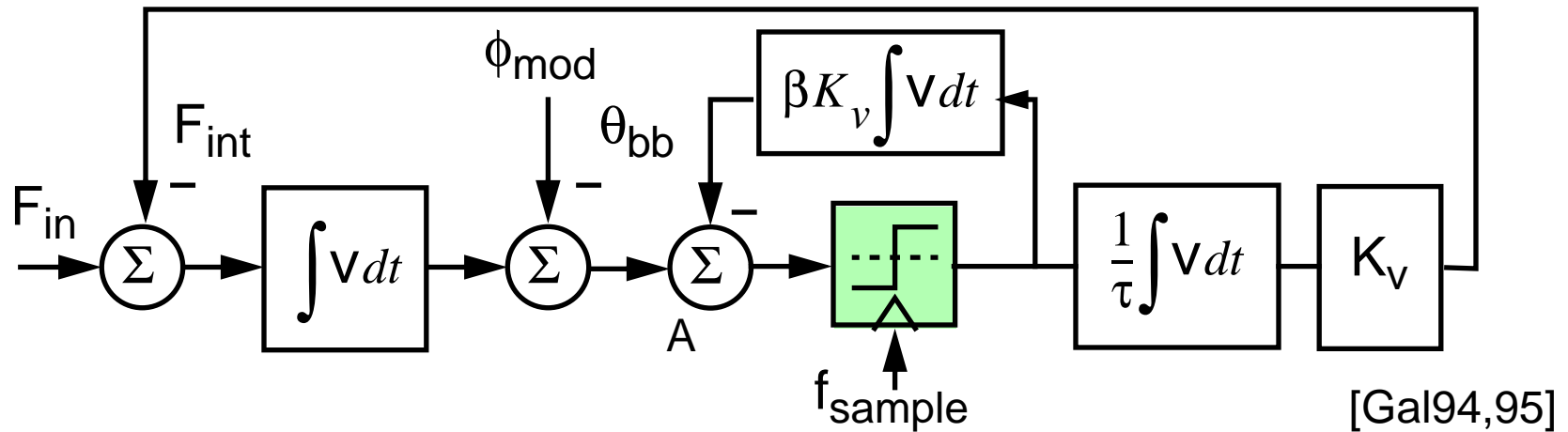
Sinusoidal phase jitter ϕ_{mod} is tracked at $\Delta\theta_1$ with a phase lag by the outer, integral loop. The resulting phase error $\Delta\theta_2$ is tracked by the inner bang-bang loop θ_{bb} to produce the final sampler phase error $\Delta\theta_3$. The PD output $V\phi$ varies with the slope of $\Delta\theta_2$ which is proportional to the instantaneous frequency error of the outer loop.

2nd-order loop: slope overload



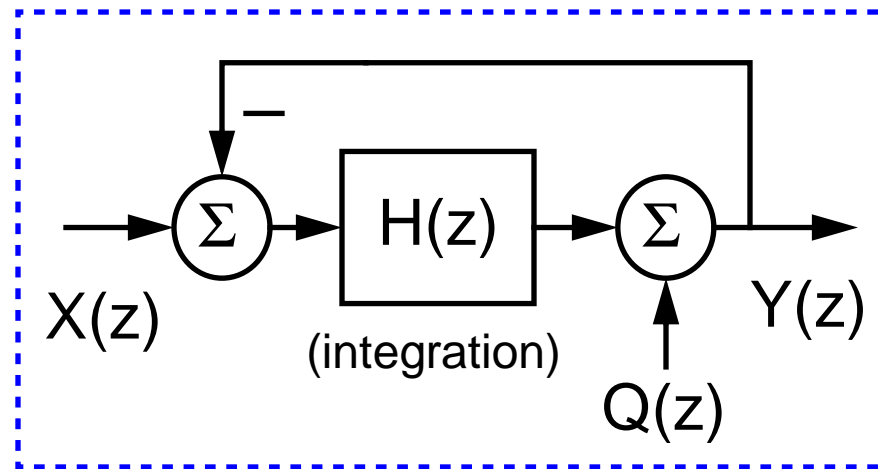
The phase modulation is increased until the instantaneous frequency error exceeds the inner loop's ability to track. Slew-rate limiting at point "A" in the inner loop θ_{bb} produces a tracking error at the sampler $\Delta\theta_3$. The loop is designed so that this situation never occurs under normal jitter tolerance conditions.

redrawing the 2nd-order loop (again)

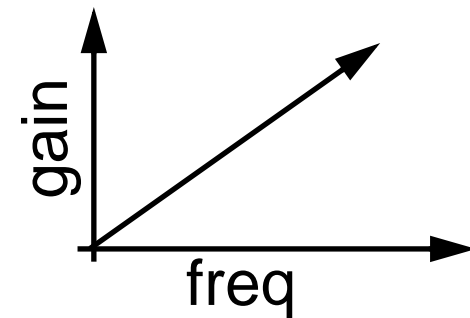
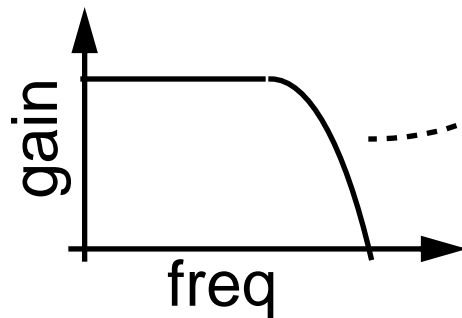


Transform the loop by pulling the integrators through the summing node “A”. Normalize update interval to 1. Let $\beta K_v V \phi = f_{bb}$. Substitute in definition for stability factor ξ . Notice that structure in blue box is a 1st order $\Delta\Sigma$ on ΔF .

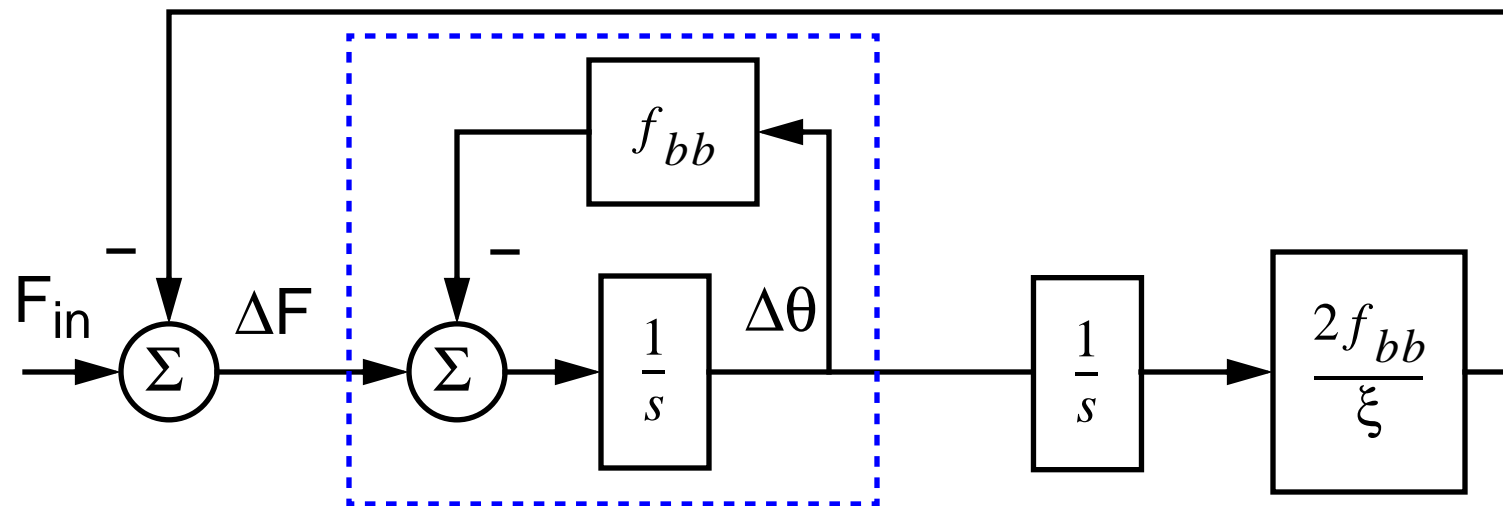
$\Delta\Sigma$ linear system analogy for bb-loop



$$Y(z) = \underbrace{\frac{H(z)}{1 + H(z)} X(z)}_{\text{gain}} + \underbrace{\frac{1}{1 + H(z)} Q(z)}_{\text{gain}}$$



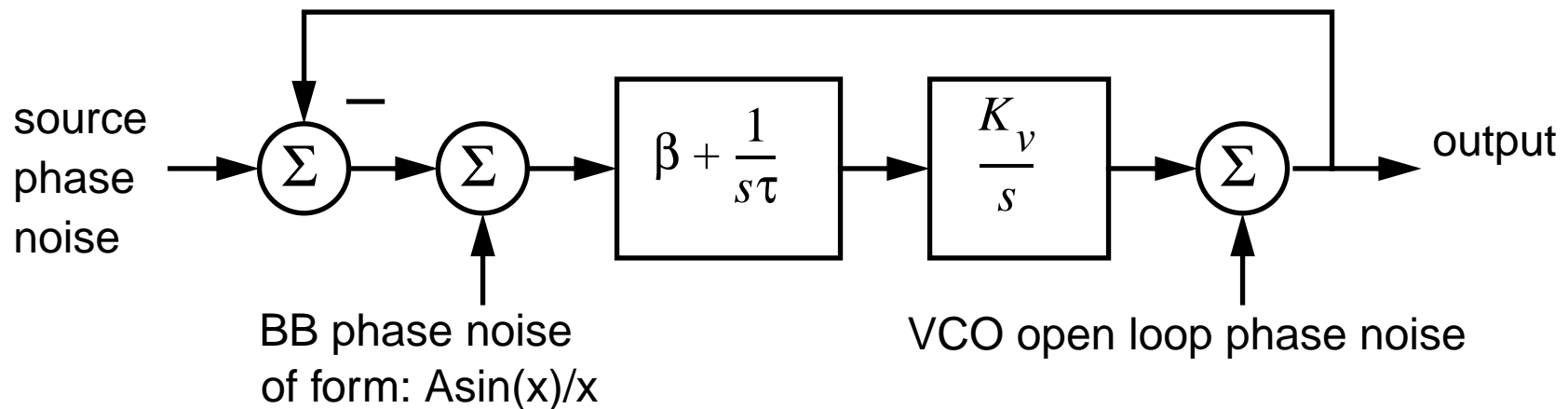
solve for slope overload



- Slew rate limiting occurs when $|\Delta F| > f_{bb}$
- Maximum input phase modulation in UI, normalized to $\Delta\theta_{bb}$ is $\left(s^2 + s + \frac{2}{\xi}\right) / (s^3 + s^2)$.
- Can be used to compute jitter tolerance.

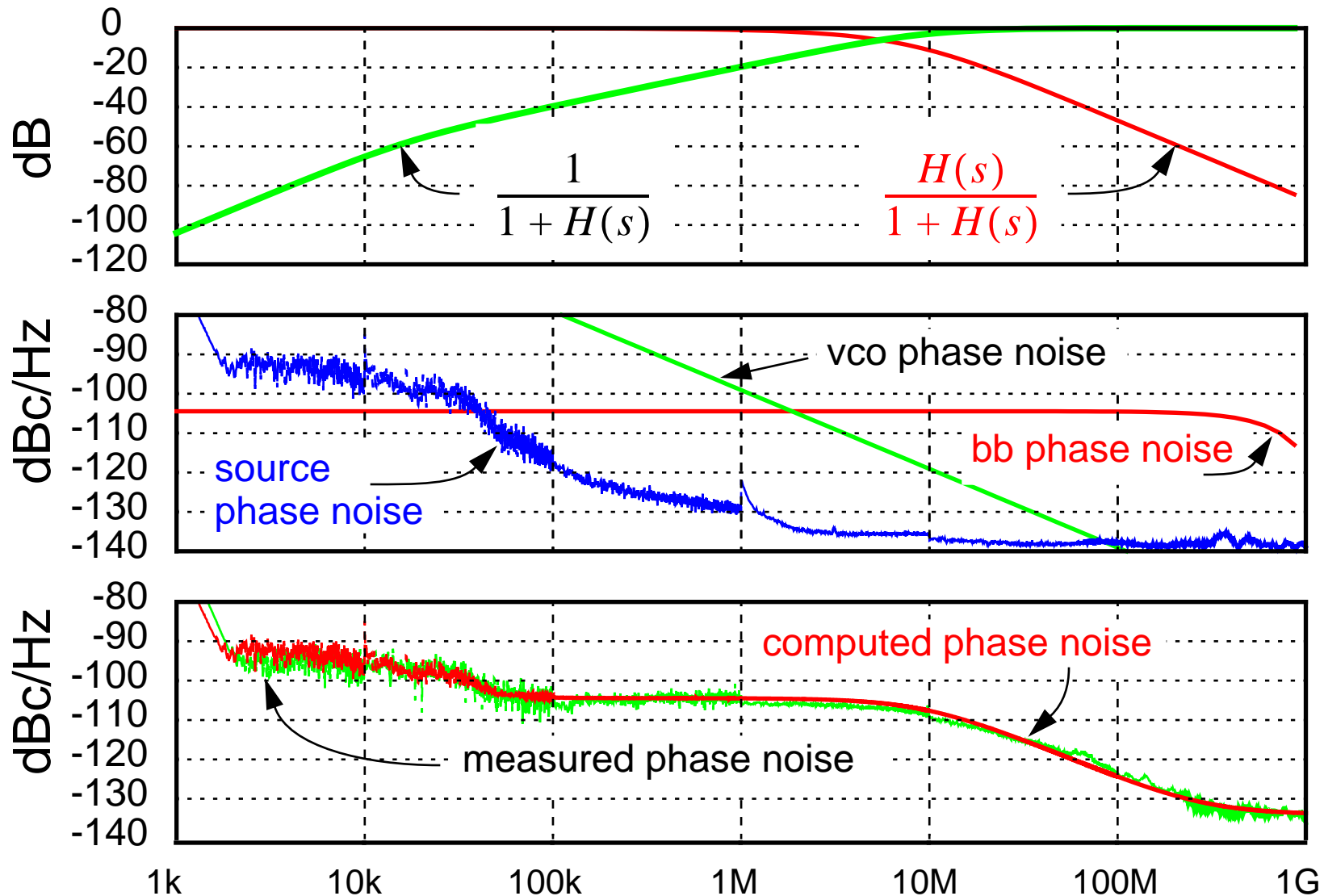
jitter generation in frequency-domain

- $\Delta\Sigma$ approximation justifies replacing BB phase detector with a noise source.
- Combine total loop phase noise by combining each phase noise source in RMS fashion.



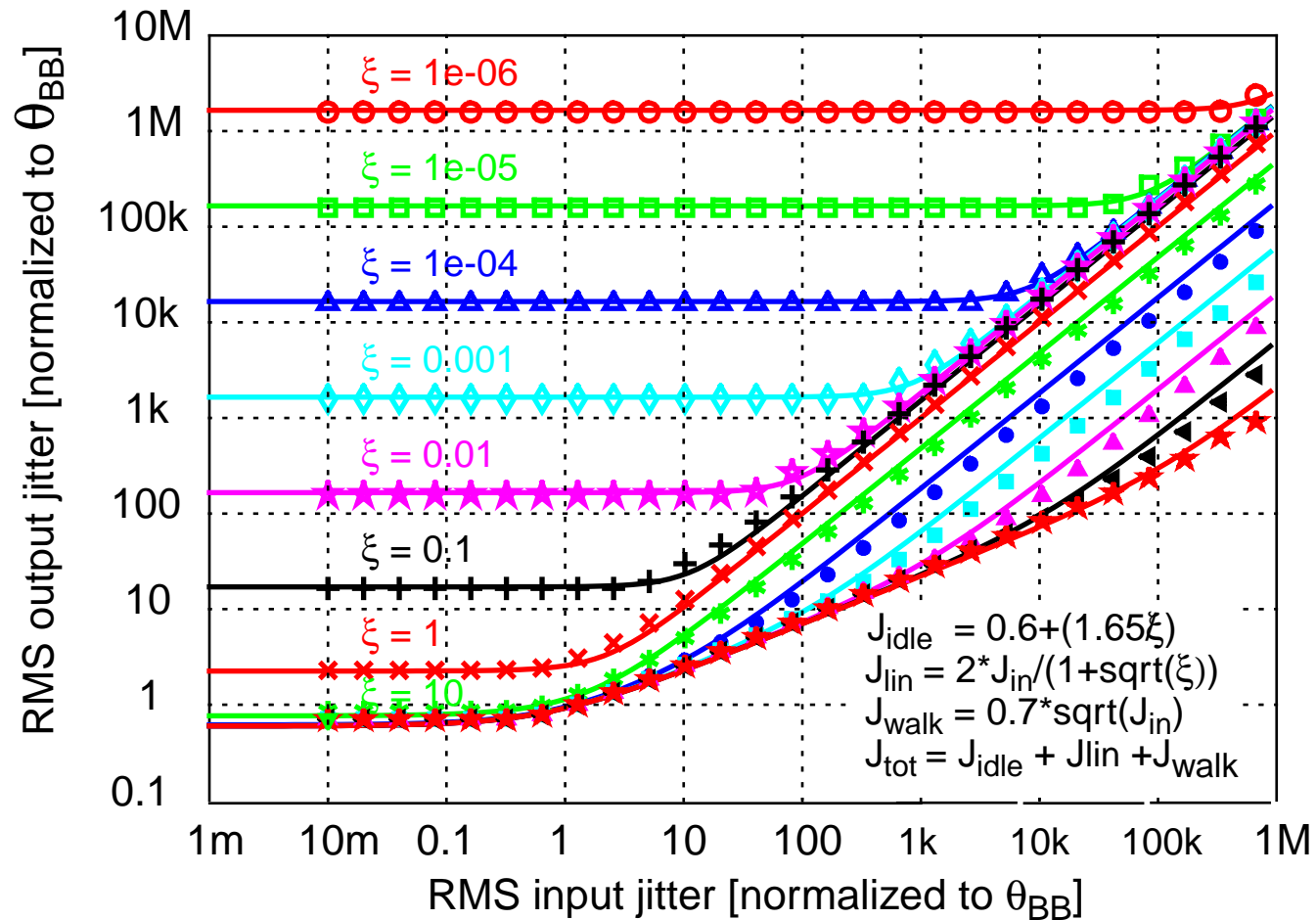
$$H(s) = \frac{K_v}{s} \left(\beta + \frac{1}{s\tau} \right)$$

example jitter generation calculation



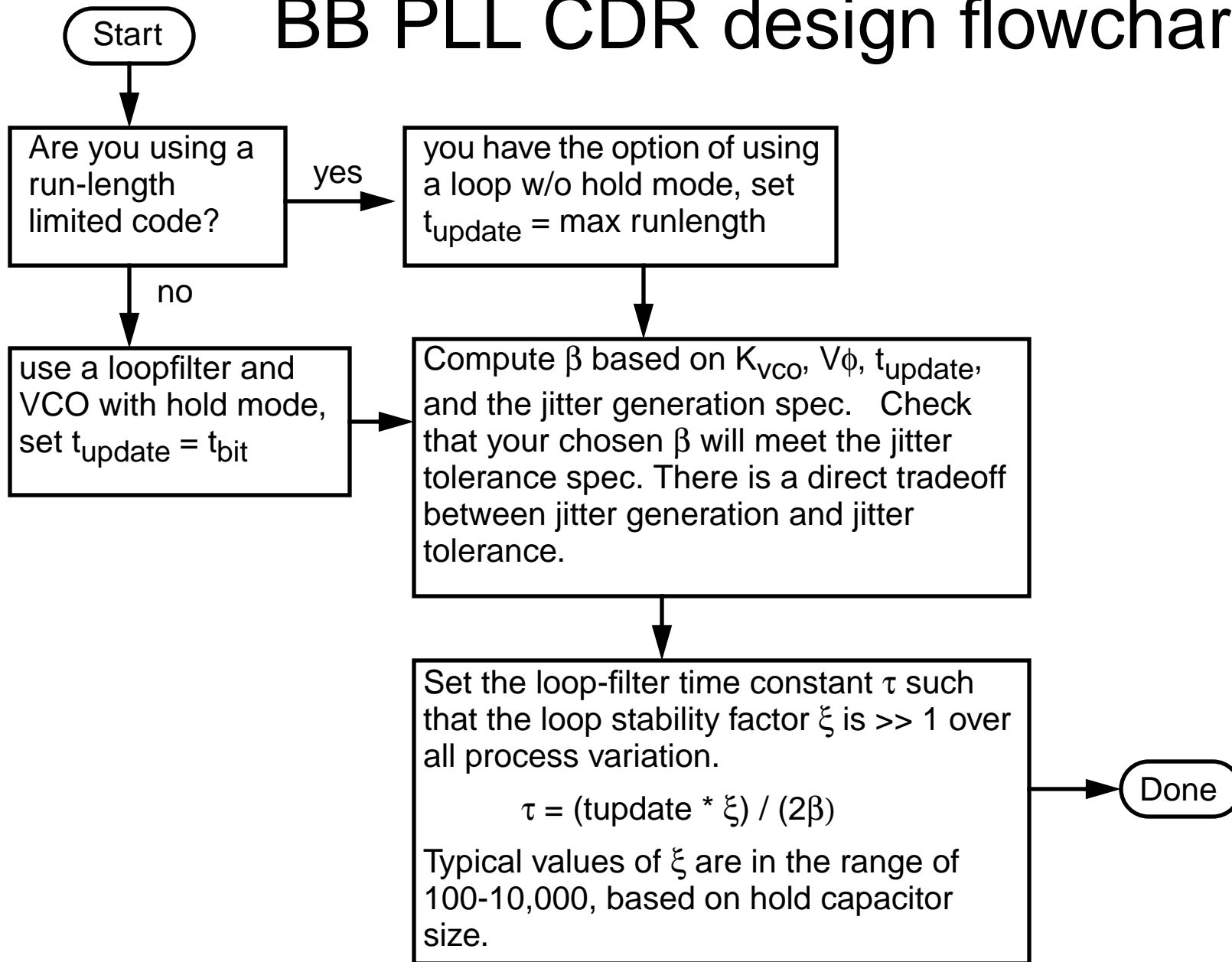
see [WSY97]: $f_{vco}=2.488$ GHz, $f_{bb} = 6$ MHz, $\xi=32000$, $t_{update}=400$ ps.

gaussian jitter generation & gain vs ξ



Simulation is for a non-tristated loop, $p_{transition} = 100\%$, with 10^8 timesteps per point. High stability-factor loops have RMS output jitter equal to the square root of the input jitter!

BB PLL CDR design flowchart



Summary

A lot of complexity for a “simple” system...

It's more of an art than a science

After understanding:

- the components,
 - the block diagrams,
 - the problems and the attempted solutions,
 - and the unique needs for your application,
- you'll be well equipped to craft an artful solution.

References

Clock and data recovery is a complex field. Any single presentation can only act as an introduction to the field. This eclectic collection of serial data communication references includes papers on signal degradation mechanisms, jitter measurement, phase locked loop design, simulation techniques, multiplexers and demultiplexers, and coding theory.

Every new application comes with a unique set of constraints and requirements, requiring an artful combination of techniques to be optimally addressed. I can't recommend anything better to the newcomer to this field than to read through the literature and internalize the many different techniques that exist.

Keywords appear in curly braces {}. Papers in **Boldface** appear on the short course CDROM in PDF format.

- [AFD87] **Andrews, G. E., D. C. Farley, S. H. Dravitz, A. W. Schelling, P. C. Davis and L. G. McAfee, A 300Mb/s Clock Recovery and Data Retiming System, *ISSCC Digest of Technical Papers*, 1987, 188-189. {SAW Filter Clock Recovery with emphasis on phase alignment problem}.**
- [Ale75] **Alexander, J. D. H., Clock Recovery from Random Binary Signals, *Electronics Letters* 11, 22 (30th October 1975), 541-542. {binary quantized phase detector}.**
- [Arm83] Armitage, C. B., SAW Filter Retiming in the AT&T 432 Mb/s Lightwave Regenerator, *Conference Proceedings: AT&T Bell Labs., Holmdel, NJ, USA*, September 3-6, 1984, 102-103. {matches tempco of SAW to tempco of electronics.}
- [Baa86] Baack, C., Optical Wide Band Transmission Systems, *CRC Press Inc.*, 1986. {example of PLL for clock recovery}.
- [BaD93] **Banu, M. and A. Dunlop, A 660Mb/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ data and Burst-Mode Transmission, *ISSCC Digest of Technical Papers*, February 1993, 102-103. {burst-mode gated VCO}.**
- [BBI94] Boudreau, P. E., W. C. Bergman and D. R. Irvin, Performance of a cyclic redundancy check and its interaction with a data scrambler, *IBM J. Res. Develop.* 38, 6 (November 1994), 651-658. {CRC theory Scrambler Error multiplication}
- [Buc92] Buchwald et al., A., A 6GHz Integrated Phase-Locked Loop using AlGaAs/GaAs Heterojunction Bipolar Transistors, *ISSCC Digest of Technical Papers*, 1992, 98,99,253. {Frequency multiplying ring oscillator}.
- [Byr63] Byrne et al., C. J., Systematic Jitter in Chain of Digital Regenerators, *The Bell System Technical Journal*, November 1963, 2679. {clock extraction by filtering}.
- [Car56] Carter, R. O., Low-Disparity Binary Coding System, *Electronics Letters* 1, 3 (May, 1956), 67-68. {conditional inversion data encoding disparity}.

- [CCI90] CCITT, Digital Line systems based on the synchronous digital hierarchy for use on optical fiber cables, *CCITT G.958*, 1990. {SONET Payload test patterns regenerator scrambling}.
- [ChB97] **Chen, D. and M. O. Baker, A 1.25 Gb/s, 460mW CMOS Transceiver for Serial Data Communication, *ISSCC Digest of Technical Papers*, February 1997, 242- 243,465. {CDR only, 10-phase bang-bang ATB loop, in 6e9 Ft 0.5um CMOS, 12.25 mm² 0.460 Watts}.**
- [Cho92] Chona, F. M. R., Draft Standard, SONET inter-office and intra-office line jitter re., *TIXI.3*, May 11, 1992. {Standards SONET jitter}.
- [Co94] Co, R. S. and J. H. M. Jr., Optimization of Phase-Locked Loop Performance in Data Recovery Systems, *IEEE Journal of Solid State Circuits* 29, 9 (September 1994), 1022-1034. {optimum design of CDR loops with linear PD}.
- [Con84] **Connor et al., P. O., A Monolithic Multigigabit/Second DCFL GaAs Decision Circuit, *IEEE Electron Device Letters EDL-5*, 7 (July 1984), 226-227. {GaAs Fet decision circuit example}.**
- [Cor79] Cordell et al., R. R., A 50MHz Phase and Frequency Locked Loop, *IEEE Journal of Solid State Circuits SC-14*, 6 (December 1979), 1003-1009. {quadricorrellator phase detector, Tunable LC Oscillator}.
- [Den88] Den Dulk, R. C., Digital Fast Acquisition Method for Phase-Lock Loops, *Electronics Letters* 24, 17 (18th August 1988), 1079-1080. {2 order of magnitude locking speed-up with fancy slip detector & charge pump}.
- [DeV91] DeVito et al., L., A 52 MHz and 155MHz Clock-Recovery PLL, *ISSCC Digest of Technical Papers*, February 13-15, 1991, 142, 143, 306. {multivibrator example, Negative resistor chargepump, rotational freq.det.}.
- [DNG91] **DeVito, L., J. Newton, R. Goughwell, J. Bulzacchelli and F.Benkley, A 52MHz and 155 MHz Clock-Recovery PLL, *ISSCC Digest of Technical Papers*, February 1991, 142-143,306. {CDR only, 1-phase rotational linear loop, in 3.5e9 Ft Bipolar, 15.028 mm² 0.575 Watts}.**
- [Dra92] Dravida, S., Error Control Aspects of High Speed Networks, *Infocom*, 1992, 272-281. {CRC performance with SONET self-synchronous scrambler}.
- [DR78] D'Andrea, N. A. and F. Russo, A Binary Quantized Digital Phase Locked Loop: A Graphical Analysis, *IEEE Transactions on Communications COM-26*, 9 (September 1978), 1355-1364. {Analysis of BB loop}.
- [EnA87] Enam, S. K. and A. A. Abidi, Decision and clock Recovery Circuits for Gigahertz Optical Fiber Receivers in Silicon NMOS, *Journal of Lightwave Technology LT-5*, 3 (March 1987), 367-372. {MOS tunable monolithic ring oscillator example - Some clever circuit ideas for gigabit rates}.
- [EnA92] **Enam, S. K. and A. A. Abidi, MOS Decision and Clock Recovery Circuits for Gb/s Optical-Fiber Receivers, *ISSCC Digest of Technical Papers*, 1992, 96,97,253. {quadratic phase detector} {MOS decision circuit example}.**
- [EWS95] **Ewen, J. F., A. X. Widmer, M. Soyuer, K. R. Wrenner, B. Parker and H. A. Ainspan, Single-Chip 1062Mbaud CMOS Transceiver for Serial Data Communication, *ISSCC Digest of Technical Papers*, February 1995, 32-33,336. {TX/RX Mux/demux, 2-phase bang-bang, data samples clock loop, in 6.6e9 Ft 0.45um CMOS, 17.55 mm² 1.2 Watts}.**
- [FHH84] Faulkner, D. W., I. Hawker, R. J. Hawkins and A. Stevenson, An Integrated Regenerator for High Speed Optical Fiber Transmission Systems, *IEE Conference Proceedings* (November 30 - December 1, 1983) 8-13. {uses rectifier/SAW combo}.
- [FLS63] Feynman, R., R. B. Leighton and M. Sands, *The Feynman Lectures on Physics*, Addison-Wesley Publishing Company, 1963. {Short, simple presentation of timestep simulator for planetary motion, same principles can be used to write a simple pll simulator}.

- [FMW97] **Fiedler, A., R. Mactaggart, J. Welch and S. Krishnan, A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis, *ISSCC Digest of Technical Papers 40* (February 6-8 1997), 238,239,464. {transmit pre-emphasis, skin loss equalizer, CDR 1:10 DEMUX, 10-phase bang-bang ATB loop, in 6e9 Ft 0.5um CMOS, 4 mm² 0.45 Watts}.**
- [Gal94] Galton, I., Higher-order Delta-Sigma Frequency-to-Digital Conversion, *Proceedings of IEEE International Symposium on Circuits and Systems* (May 30 - June 2, 1994) 441-444 {Delta-Sigma BB loops phase tracking frequency digitalization PLL}.
- [Gal95] **Galton, I., Analog-Input Digital Phase-Locked Loops for Precise Frequency and Phase Demodulation, *Transactions on Circuits and Systems-II: Analog and Digital Signal Processing* 42, 10 (October 1995), 621-630. {good discussion of delta-sigma analysis of BB PLL's}.**
- [Gar79] Gardner, F. M., *Phaselock Techniques, Second Edition*, John Wiley and Sons, Inc., 1979. {example of using exor-gate to generate clock component from NRZ data}.
- [GHW94] Guo, B., A. Hsu, Y. Wang and J. Kubinec, 125Mb/s CMOS All-Digital Data Transceiver Using Synchronous Uniform Sampling, *ISSCC Digest of Technical Papers*, February 1994, 112-113. {TX/RX, 1-phase ATB with digital phase adjustment loop, in 3.75e9 Ft 0.8um CMOS, 6.38 mm² 0.175 Watts}.
- [Gla85] Glance, B. S., New Phase-Lock Loop Circuit Providing Very Fast Acquisition Time, *IEEE Transactions on Microwave Theory and Techniques MTT-33*, 9 (September 1985), 747-754. {adds non-linear time constant to speed PLL acquisition by 2 orders of mag.}.
- [GMP78] Gruber, J., P. Marten, R. Petschacher and P. Russer, Electronic Circuits for High Bit Rate Digital Fiber Optic Communication Systems, *IEEE Transactions on Communications COM-26*, 7 (July 1978), 1088-1098.
- [Gol82] Golomb, S. W., Shift Register Sequences, *Aegean Park Press*, 1982. {classic text on Pseudo-Random sequence generation, ISBN:0-89412-048-4}
- [Gri69] Griffiths, J. M., Binary Code Suitable for Line Transmission, *Electronics Letters* 5, 4 (February 20, 1969), 79-81. {5b/6b encoding example}.
- [GSS00a] Greshishchev, Y. M., P. Schvan, J. L. Showell, M. Xu, J. J. Ojha and J. E. Rogers, A Fully Integrated SiGe Receiver IC for 10Gb/s Data Rate, *ISSCC Digest of Technical Papers*, February 2000, 52-53,447. {CDR DEMUX BIST, 1-phase bang-bang loop, in 50e9 Ft SiGe, 20.25 mm² 4.5 Watts}.
- [GSS00b] **Greshishchev, Y. M., P. Schvan, J. L. Showell, M. Xu, J. J. Ojha and J. E. Rogers, A Fully Integrated SiGe Receiver IC for 10-Gb/s Data Rate, *IEEE Journal of Solid State Circuits* 35, 12 (December 2000), 1949-1957. {CDR DEMUX BIST, 1- phase bang-bang loop, in 50e9 Ft SiGe, 20.25 mm² 4.5 Watts}.**
- [GTL99] **Gu, R., J. M. Tran, H. Lin, A. Yee and M. Izzard, A 0.5-3.5Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver, *ISSCC Digest of Technical Papers*, February 1999, 352-353,478. {TX/RX MUX/DEMUX BIST, 10-phase bang-bang ATB loop, in 10.7e9 Ft 0.28um CMOS, 1 mm² 0.250 Watts}.**
- [Gup75] Gupta, S. C., Phase-Locked Loops, *Proceedings of the IEEE* 63, 2 (February 1975), 291-306. {Good systematic outline survey of communication-type PLL's}.
- [Hau91a] Hauenschild et al., J., A Silicon Bipolar Decision Circuit Operating up to 15Gb/s, *IEEE Journal of Solid State Circuits* 26, No.11 (November 1991), 1734-1736. {Si bipolar decision circuit example}.
- [Hau91b] Hauser, M. W., Principles of Oversampling A/D Conversion, *J. Audio Eng. So. Vol 39*, 1/2 (Jan/February 1991), 3-26. {excellent tutorial on Delta Sigma AD, Oversampling, noiseshaping}.

- [HDM96] **Hauenschild, J., C. Dorshcky, T. W. Mohrenfels and R. Seitz, A 10Gb/s BiCMOS Clock and Data Recovery 1:4-Demultiplexer in a Standard Plastic Package with External VCO, *ISSCC Digest of Technical Papers*, February 1996, 202-203,445. {CDR 4:1 DEMUX, 2-phase bang-bang ATB loop, in 16e9 Ft BiCMOS, 5.29 mm² 0.450 Watts}.**
- [HeS88] Hein, J. P. and J. W. Scott, z-Domain Model for Discrete-Time PLL's, *IEEE Transactions on Circuits and Systems* 35, 11 (November 1988), 1393-1400. {good discussion of using z-transforms in PLL analysis}.
- [Hog85] **Hogge, Jr., C. R., A Self Correcting Clock Recovery Circuit, *IEEE Transactions on Electron Devices ED-32*, 12 (December 1985), 2704-2706. {Original Hogge detector, interesting phase detector idea...}.**
- [Hor92] Hornak, T., Interface Electronics for Fiber Optic Computer Links, *Intensive Course on Practical Aspects in Analog IC Design*, Lausanne, Switzerland, June 29-July 10, 1992. {Excellent overview of components for serial optical data transmission}.
- [HuG93] **He, T. and P. Gray, A Monolithic 480 Mb/s AGC/Decision/Clock Recovery Circuit in 1.2 um CMOS, *IEEE Journal of Solid State Circuits* 28, 12 (Dec. 1993) 1314-20 {CDR only, 8-phase linear ATB loop, in 2.4e9 Ft 1.2um CMOS, 9 mm² 0.9 Watts}.**
- [IsA94a] **Ishihara, N. and Y. Akazawa, A Monolithic 156Mb/s Clock and Data-Recovery PLL Circuit using the Sample-and-Hold Technique, *IEEE Journal of Solid State Circuits* 29, 12 (December 1994), 1566-1571. {CDR only, 1-phase linear 90-degree delayed data + narrow pulses loop, in 16e9 Ft Bipolar, 8.4 mm² 0.320 Watts}.**
- [IsA94b] Ishihara, N. and Y. Akazawa, A Monolithic 156Mb/s Clock and Data-Recovery PLL Circuit using the Sample-and-Hold Technique, *ISSCC Digest of Technical Papers*, February 1994, 110-111,318. {CDR only, 1-phase linear 90-degree delayed data + narrow pulses loop, in 16e9 Ft Bipolar, 8.4 mm² 0.320 Watts}.
- [Kas85] Kasper et al., B. L., SAGM Avalanche Photodiode Optical Receiver for 2 Gbit/s and 4 Gbit/s, *Electronic Letters* 21, 21 (10th October 1985), 982-984. {eye diagram}.
- [KWG94] Kim, B., T. C. Weigandt and P. R. Gray, PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design, *ISCAS proceedings*, May 30 - June 2, 1994, 31-34. {Excellent and Intuitive discussion of Jitter in Ring Oscillators}.
- [Lai90] Lai, B., Decision Circuit Lowers Transmission Bit Error Rates, *Microwaves and RF*, July 1990, 118- 122. {Si bipolar decision circuit example}.
- [Lam93] Lam, V. M. T., Microwave Oscillator Phase Noise Reduction Using Negative Resistance Compensation, *Electronics Letters* 29, 4 (February 18th, 1993), 379-340. {Leeson negative resistance phase noise second harmonic IC}.
- [Lar99] **Larsson, P., A 2-1600MHz 1.2-2.5V CMOS Clock- Recovery PLL with Feedback Phase-Selection and Averaging Phase-Interpolation for Jitter Reduction, *ISSCC Digest of Technical Papers*, February 1999, 356-357. {CDR only, 1-phase bang- bang with digital phase shifter loop, in 12e9 Ft 0.25um CMOS, 0.036 mm² 0.072 Watts}.**
- [LaW91] Lai, B. and R. C. Walker, A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit, *ISSCC Digest of Technical Papers* 34 (February 13-15, 1991), 144,145. {binary quantized phase detector}.
- [LeB92a] **Lee, T. H. and J. F. Bulzacchelli, A 155MHz Clock Recovery Delay- and Phase-Locked Loop, *ISSCC Digest of Technical Papers*, February 1992, 160- 161,272. {CDR only, 1-phase rotational linear loop, in 3.5e9 Ft Bipolar, 10.75 mm² 0.364 Watts}.**
- [LeB92b] **Lee, T. H. and J. F. Bulzacchelli, A 155MHz Clock Recovery Delay- and Phase-Locked Loop, *IEEE Journal of Solid State Circuits* 27, 12 (December 1992), 1736-1746. {CDR only, 1-phase linear 90- degree delayed data + narrow pulses loop, in 16e9 Ft Bipolar, 8.4 mm² 0.320 Watts}.**

- [LeS88] Leonowich, R. H. and J. M. Steininger, A 45-MHz CMOS phase/frequency-locked loop timing recovery circuit, *ISSCC Digest of Technical Papers*, February 1988, 14. {CDR only, 1-phase linear (narrow pulse), rotation frequency detector loop, in 1.65e9 Ft 1.75um CMOS, 3 mm².250 Watts}.
- [LiC81] Lindsey, W. C. and C. M. Chie, A Survey of Digital Phase-Locked Loops, *Proceeding of the IEEE* 69, 4 (April 1981), 410-431. {Presents a good taxonomy of digital PLLs}.
- [LYK96] Lee, I., C. Yoo, W. Kim, S. Chai and W. Song, A 622Mb/s CMOS Clock Recovery PLL with Time- Interleaved Phase Detector Array, *ISSCC Digest of Technical Papers*, February 1996, 198-199,444. {CDR DEMUX, 8-phase bang-bang ATB loop, in 3.75e9 Ft 0.8um CMOS, 0.72 mm² 0.200 Watts}.
- [Mac87] MacDougall, M. H., *Simulating Computer Systems - Techniques and Tools*, The MIT Press, Cambridge, Massachusetts, 1987. {description and source code for event driven simulator}.
- [MCC01] Momtaz, A., J. Cao, M. Caresosa, A. Hairapitian, D. Chung, K. Vakilian, M. Green, B. Tan, K. Jen, I. Fujimori, G. Gutierrez, Y. Cai, S. Ueno, K. Watanabe, T. Kato, T. Shinohara, K. Mikami, T. Hashimoto, A. Takai, K. Washio, R. Takeyar and T. Harada, A Single-Chip 10Gb/s Transceiver LSI using SiGe SOI/BiCMOS, *ISSCC Digest of Technical Papers*, February 2001, 82-83,435. {TX/RX MUX/DEMUX BIST, 1-phase linear rotational sample-hold loop, in 90e9 Ft SiGe CMOS, 29.68 mm² 2.6 Watts}.
- [McG90] McGaughey, J. T., Convert NRZ format to Biphasic, *Electronic Design*, April 12, 1990, 86. {biphase example}.
- [MPA00] Meghelli, M., B. Parker, H. Ainspan and M. Soyuer, A SiGe BiCMOS 3.3V Clock and Data Recovery Circuit for 10Gb/s Serial Transmission Systems, *ISSCC Digest of Technical Papers*, February 2000, 56-57. {CDR only, 1-phase bang-bang loop, in 45e9 Ft, 6 mm² 0.42 Watts}.
- [MSS99] Morikawa, T., M. Soda, S. Shiori, T. Hashimoto, F. Sato and K. Emura, A SiGe Single-Chip 3.3V Receiver IC for 10Gb/s Optical Communication System, *ISSCC Digest of Technical Papers*, February 1999, 380-381,481. {CDR TIA only, 1-phase linear Hogge loop, in 60e9 Ft SiGe, 6 mm² 0.66 Watts}.
- [OFC84] O'Connor, P., P. G. Flahive, W. Clemetson, R. L. Panock, S. H. Wemple, S. C. Shunk and D. P. Takahashi, A Monolithic Multigigabit/ Second DCFL GaAs Decision Circuit, *IEEE Electron Device Letters EDL-5*, 7 (July 1984),. {2.4 GHz ED GaAs Mesfet Flip-flop w/ input buffer amp}.
- [Ofe89] Ofek, Y., The Conservative Code for Bit Synchronization, *IEEE Transactions on Communications*, 1989. {conserves transition number, uses divider for clock recovery}.
- [OhT83] Ohta, N. and T. Takada, High Speed GaAs SCFL Monolithic Integrated Decision Circuit for Gb/s Optical Repeaters, *Electronics Letters*, September 1983. {GaAs Decision Circuit}.
- [Par89] Park et al., M. S., Novel Regeneration Having Simple Clock Extraction and Automatic Phase Controlled Retiming Circuit, *Electronic Letters* 25 (January 1989), 83-84. {clock extraction by filtering}.
- [Pet88] Petrovic, R., Low Redundancy Optical Fiber Line Code, *Journal of Optical Communication* 9, 3 (1988), 108-111. {13B/14B code design}.
- [PLS92] Pottbacker, A., U. Langmann and H. Schreiber, A Si bipolar phase and frequency detector IC for clock extraction up to 8Gb/s, *IEEE Journal of Solid State Circuits* 27, 12 (December 1992), 1747-1751. {linear quadrature phase/frequency detector}.

- [PoL94a] **Pottbacker, A. and U. Langmann, An 8GHz Silicon Bipolar Clock-Recovery and Data-Regenerator IC, *IEEE Journal of Solid State Circuits* 29, 12 (December 1994), 1572-1576. {CDR only, 1-phase linear loop, in 25e9 Ft Bipolar, 3.06 mm² 2.25 Watts}.**
- [PoL94b] Pottbacker, A. and U. Langmann, An 8GHz Silicon Bipolar Clock-Recovery and Data-Regenerator IC, *ISSCC Digest of Technical Papers*, February 1994, 116-117,320. {CDR only, 1-phase linear loop, in 25e9 Ft Bipolar, 3.06 mm² 2.25 Watts}.
- [RaO91] **Ransijn, H. and P. O'Connor, A PLL-Based 2.5-Gb/s GaAs Clock and Data Regenerator IC, *JSSC* 26, 10 (October 1991), 1345-1353. {Rotational frequency detector, Limiting Amp, Jitter Transfer Measurement}.**
- [Raz96a] B. Razavi, ed., *Monolithic phase-locked loops and clock recovery circuits: theory and design*, IEEE Press, 1996. {A volume of selected reprints with bibliography}.
- [Raz96b] Razavi, B., Monolithic Phase-Locked Loops, *ISSCC Tutorial*, San Francisco, CA, February 7, 1996. {Good overview of non-data-driven PLL theory}.
- [Raz96c] **Razavi, B., A 2.5-Gb/s 15-mW Clock Recovery Circuit, *IEEE Journal of Solid State Circuits* 31, 4 (April 1996), 472-480. {dual loop phase frequency quadricorrelator}.**
- [RCF84] Rosenberg, R. L., C. Chamzas and D. A. Fishman, Timing Recovery with SAW Transversal Filters in the Regenerators of Undersea Long-Haul Fiber Transmission Systems, *Journal of Lightwave Technology LT-2*, 6 (December 1984), 917-925. {discusses jitter accumulation}.
- [RDP01] **Reinhold, M., C. Dorschky, F. Püllela, E. Rose, P. Mayer, P. Paschke, Y. Baeyens, J. Mattia and F. Kunz, A Fully-Integrated 40Gb/s Clock and Data Recovery / 1:4 DEMUX IC in SiGe Technology, *ISSCC Digest of Technical Papers*, February 2001, 84-85,435. {CDR DEMUX, 4-phase ATB loop, in 72e9 Ft SiGe HBT, 9 mm² 5.4 Watts}.**
- [ReG73] Reddy, C. P. and S. C. Gupta, A Class of All-Digital Phase Locked Loops: Modeling and Analysis, *IEEE Transactions on industrial Electronics and Control Instrumentation IECI-20*, 4 (November 1973), 239-251. {discusses of binary-quantized phase detection}.
- [RHF90] Ross, F. E., J. R. Hamstra and R. L. Fink, FDDI - A LAN among MANs, *ACM Computer Communications Review*, July 1990, 16-31. {4b/5b encoding example}.
- [RoM77] Roza, E. and P. W. Millenaar, An Experimental 560 MBit/s Repeater with Integrated Circuits, *IEEE Transactions on Communications COM-25*, 9 (September 1977),. {coax-based. good comparison of PLL vs filter-type clock extraction}.
- [Ros84] Rosenberg et al., R. L., Timing Recovery with SAW Transversal filters in the Regenerators of Undersea Long-haul Fiber Transmission Systems, *IEEE Journal of Lightwave Technology LT-2*, 6 (December 1984), 917-925. {clock extraction by SAW}.
- [Ros85] Ross, F. E., An Overview of FDDI: the Fiber Distributed Data Interface, *IEEE Journal on Selected Areas in Communications* 7, 7 (September 1985), 1046, Table 1. {4b/5b encoding example, example of frame synch characters}.
- [Rou76] Rousseau, M., Block Codes for Optical-Fibre Communication, *Electronics Letters* 12, 18 (2nd September 1976), 478-479. {mBnB code discussion, run length limits, power spectra, 5b6b recommended}.
- [RuG91] Runge, K. and J. L. Gimlett, 20Gb/s AlGaAs HBT Decision Circuit IC, *Electronics Letters* 27, 25 (5th December 1991), 2376-2378. {GaAs HBT decision circuit example}.
- [Run91] Runge et al., K., Silicon Bipolar Integrated Circuits for Multi-Gb/s Optical Communication Systems, *IEEE Journal on Selected Areas in Communications* 9, 5 (June 1991), 640. {Si bipolar decision circuit example}.
- [San82] Sandera, L., Improve Datacomm Links by Using Manchester Code, *EDN*, February 17, 1982, 155-162. {manchester coding example}.

- [Shi87] Shin et al., D., Selfcorrecting Clock Recovery Circuit with Improved Jitter Performance, *Electronics Letters* 23, 3 (29th January 1987), 110-111. {Improved Hogge detector}.
- [SHL99] Scheytt, C., G. Hanke and U. Langmann, A 0.155-, 0.622-, and 2.488-Gb/s Automatic Bit-Rate Selecting Clock and Data Recovery IC for Bit-Rate Transparent SDH Systems, *IEEE Journal of Solid State Circuits* 34, 12 (December 1999), 1935-1943. {quadrature p/f detector, delay-interpolated ring oscillator}.
- [SoA93] Soyuer, M. and H. A. Ainspan, A Monolithic 2.3 Gb/s 100mW Clock and Data Recovery Circuit, *ISSCC Digest of Technical Papers*, February 1993, 158- 159,282. {CDR only, 1-phase bang-bang data triggered loop, in 30e9 Ft Bipolar, 1.3 mm² 0.100 Watts}.
- [SyA86] Syed, K. E. and A. A. Abidi, Gigahertz Voltage Controlled Oscillator, *Electronics Letters* 22 (June 5, 1986), 677-679. {MOS tunable monolithic ring oscillator example}.
- [TrV89] Trischitta, P. R. and E. L. Varma, *Jitter in digital transmission systems*, Artech House, Inc., 1989. {good overview of jitter (textbook) ISBN 0-89006-248-X}.
- [UWK01] Ueno, S., K. Watanabe, T. Kato, T. Shinohara, K. Mikami, T. Hashimoto, A. Takai, K. Washio, R. Takeyar and T. Harada, A Single-Chip 10Gb/s Transceiver LSI using SiGe SOI/BiCMOS, *ISSCC Digest of Technical Papers*, February 2001, 82-83,435. {TX/RX MUX/DEMUX BIST, 1-phase linear rotational sample-hold loop, in 90e9 Ft SiGe CMOS, 29.68 mm² 2.6 Watts}.
- [Wal89] Walker, R. C., Fully Integrated High Speed Voltage Controlled Ring Oscillator, *U.S. Patent 4,884,041*, Granted Nov. 28, 1989. {Si bipolar tunable monolithic ring oscillator example}.
- [WaN99] Wang, H. and R. Nottenburg, A 1Gb/s CMOS Clock and Data Recovery Circuit, *ISSCC Digest of Technical Papers*, February 1999, 354-355,477. {CDR only, 1-phase analog track-hold + rotational fd loop, in 6e9 Ft 0.5um CMOS, 7.29 mm² 0.300 Watts}.
- [WBS90] Wallace, P., R. Bayruns, J. Smith, T. Laverick and R. Shuster, A GaAs 1.5Gb/s Clock Recovery and Data Retiming Circuit, *ISSCC Digest of Technical Papers*, February 1990, 192-193. {CDR only, 1-phase delay & multiply w/SAW loop, in 20e9 Ft 0.5um GaAs MESFET, 2 mm² 0.75 Watts}.
- [WBS94] Wang, Z., M. Berroth, J. Seibel, P. Hofmann, A. Hulsmann, Kohler, B. Raynor and J. Schneider, 19GHz Monolithic Integrated Clock Recovery Using PLL and 0.3um Gate-Length Quantum-Well HEMTs, *ISSCC Digest of Technical Papers*, February 1994, 118-119. {CDR only, 1-phase linear xor of data and clock pulses loop, in 50e9 Ft 0.3um HEMT, 1.5 mm² 0.350 Watts}.
- [WHK98] Walker, R. C., K. Hsieh, T. A. Knotts and C. Yen, A 10Gb/s Si-Bipolar TX/RX Chipset for Computer Data Transmission, *ISSCC Digest of Technical Papers* 41 (February 5-7 1998), 302,303,450. {multi-phase architecture, 8-phase VCO, ft-doubler amplifier, bb-loop CDR MUX/DEMUX, 4-phase BB/ATB loop, in 25e9 Ft Bipolar, 28.6 mm² 8.5 Watts}.
- [WHY91] Walker, R. C., T. Hornak, C. Yen, J. Doernberg and K. H. Springer, A 1.5Gb/s Link Interface Chipset for Computer Data Transmission, *IEEE Journal on Selected Areas in Communications* 9, 5 (June 1991), 698-703. {binary quantized phase detector with master transition}.
- [WiF83] Widmar, A. X. and P. A. Franaszek, A DC Balanced, partitioned-Block 8B/10B Transmission Code, *IBM Journal of Research and Development* 27, 5 (September 1983), 440-451. {8b/10b encoding example - Precursor to Fiber Channel's 8B/10B code}.

- [WKG94] Weigandt, T. C., B. Kim and P. R. Gray, Analysis of Timing Jitter in CMOS Ring Oscillators, *ISCAS proceedings, May 30 - June 2, 1994*. {Excellent and Intuitive discussion of Jitter in Ring Oscillators}.
- [WSY97] Walker, R., C. Stout and C. Yen, A 2.488Gb/s Si-Bipolar Clock and Data Recovery IC with Robust Loss of Signal Detection, *ISSCC Digest of Technical Papers 40* (February 6-8 1997), 246,247,466. {training loop, loss of signal detection, bb-loop, ring oscillator}.
- [WuW92] Wu, J. and R. C. Walker, A Bipolar 1.5Gb/s Monolithic Phase Locked Loop for Clock and Data Extraction, *VLSI Circuit Symposium*, Seattle, June 3-5, 1992. {positive feedback PLL loop filter}.
- [WWS92] Walker, R., J. Wu, C. Stout, B. Lai, C. Yen, T. Hornak and P. Petruno, A 2-Chip 1.5Gb/s Bus-Oriented Serial Link Interface, *ISSCC Digest of Technical Papers 35* (February 19-21 1992), 226,227,291. {MT Code, Ring Osc binary quantized phase detector with master transition TX/RX MUX/DEMUX, 1-phase bang-bang loop, in 25e9 Ft Bipolar, 24.5 mm² 3.8 Watts}.
- [YaH96a] Yang, C. K. and M. A. Horowitz, 0.8um CMOS 2.5Gb/s Oversampled Receiver for Serial Links, *ISSCC Digest of Technical Papers*, February 1996, 200- 201,444. {CDR DEMUX, 8-phase digital 3x oversampled loop, in 3.75e9 Ft 0.8um CMOS, 9 mm² 2.25 Watts}.
- [YaH96b] Yang, C. K. and M. A. Horowitz, 0.8um CMOS 2.5Gb/s Oversampled Receiver for Serial Links, *IEEE Journal of Solid State Circuits* 31, 12 (December 1996), 2015-2023. {CDR DEMUX, 8-phase digital 3x oversampled loop, in 3.75e9 Ft 0.8um CMOS, 9 mm² 2.25 Watts}.
- [Yam80] Yamada et al., J., 1.6Gb/s Optical Receiver at 1.3um with SAW Timing Retrieval Circuit, *Electronics Letters* 16, 2 (17th January 1980), 57- 58. {clock extraction by SAW}.
- [YFW82] Yen, C., Z. Fazarinc and R. Wheeler, Time-domain skin-effect model for transient analysis of lossy transmission lines., *Proceedings of the IEEE* 70, 7 (July 1982), 750-757. {skin-effect lossy transmission line transient simulation modelling}.
- [YKI84] Yoshikai, N., K. Katagiri and T. Ito, mB1C Code and its Performance in an Optical Communication System, *IEEE Transactions on Communications COM-32*, 2 (February 1984). {uses m binary bits + one complementary bit stuffed to break runs}.
- [YTY80] Yamada, J., J. Temmyo, S. Yoshikawa and T. Kimura, 1.6 Gbit/s Optical Receiver at 1.3um with SAW Timing Retrieval Circuit, *Electronics Letters*, 1980, 57-58. {basic SAW system, with discussion of power penalty for SAW phase shifts}.