A single-inductor multiple-output buck boost converter

Richard Walker

Abstract

Modern CMOS IC's typically require several different voltages for operation. Usually a higher voltage such as 3.3 Volts is used for IO drivers and low-speed analog circuitry. A lower voltage such as 1.1 Volts is used for high density core logic for pure digital computation. In many portable applications, such a chip will need to be powered from a single source voltage, such as the 5.0 Volts provided by the USB VBUS power supply. To minimize system power, it is critical that the various chip voltages are provided by an efficient switch-mode power supply (SMPS) rather than a linear regulator. Commercially available solutions require one inductor per voltage generated. The inductors are often larger than the SMPS chip itself and can dominate the PCB area required for a solution. This paper presents a novel multi-voltage converter that requires a single inductor to generate an arbitrary number of regulated output voltages.

1 Multi-output converter topology

The proposed circuit modifies a standard boost circuit by adding a multiplexer so that multiple output circuits can be driven in a round-robin fashion.

In a switching power supply operating in continuous current mode, the current in the inductor is approximately constant. The current decreases slightly from nominal while connected to the load, and increases by the same amount when connected to the input voltage supply voltage. To first order, we can analyze the output voltage of a multi-output supply by considering the inductor as a constant current source I_0commutated between more than one output. Figure 1 shows a current source repetitively switched between n output circuits, dwelling at each output for time T_n . In a practical circuit, the inductor current droops when driving a load, so we allow for one extra time period T_{n+1} for "recharging" the inductor by connection to the input supply. The total time for each cycle is $T_0 = \sum_{k=1}^{n+1} T_k$. The duty cycle of the pulse driving each output is $D_k = T_k/T_0$.

Due to the filtering effect of the output capacitors, the average voltage at each output is a function of the duty cycles and impedances at each node

$$V_n = D_n I_0 R_n \tag{1}$$

The ratio of any two duty cycles is the ratio of the average load currents

$$\frac{D_m}{D_n} = \frac{V_m R_n}{V_n R_m} \tag{2}$$

Assuming that the system has a steady state average inductor current I_L, then we can compute the total change of current after one complete cycle. (these equations neglect the second order transient from the LC combination, and are essentially assuming an infinite filter capacitor):

$$I_L(t + T_0) = I_L(t) + \sum_{k=1}^{n} \frac{1}{L} \int (V_s - V_k) dt \tag{3}$$

For a steady state solution, the total change in I_L must equal zero

$$V_s T_{k+1} + \sum_{k=1}^{n} (V_s - V_k) T_{1k} = 0$$

Solving for T_{k+1}, the time that the inductor needs to be connected to the input power supply:

$$T_{k+1} = \sum_{k=1}^{n} T_k (\frac{V_k}{V_s} - 1) \tag{4}$$

Since T_{k+1}cannot be negative, this expression says that at least one output must be a boost output.

2 Design example

We attempt to synthesize a switching supply for the HOST end requirements for the lightning project using the above design equations. The givens are shown in table 1.

Lightning IC, USB3.0 mode		
V_s	5V	
V_1	1V	
R_1	3.16Ω	316mA @ 1V
V_2	3.3V	
R_2	25Ω	132mA @ 3.3V
V_3	20V	
R_3	178Ω	113mA @ 20V

Tab. 1: Given parameters for Lightning power supply requirements

If we arbitrarily set $T_1 = 1$, equation 2 sets T_2, T_3. $T_4$is set by equation 4. The derived numerical values for this design are given in Table 2.

	Normalized time	Duty Cycle
T_1	1.000	0.527
T_2	0.417	0.220
T_3	0.355	0.187
T_4	0.123	0.065
Total	1.895	1.000

Tab. 2: Derived parameters

3 Simulated steady state performance

An awk script was written to solve the approximate discrete difference equations to test the accuracy of the derivations above.

The resulting data shows steady state voltages of V1=0.983, V2=3.343, and V3=19.99, all within 2% of target values. The total current drawn by the (admittedly ideal) system is 0.317 amps, well within the design target and the USB VBUS current limit.

4 Controlling the loop under dynamic load changes

The derivation and simulation results are encouraging. What remains is the design of a workable control loop for the system. Two possibilities are being explored. A simple bang-bang loop has been shown to be able to stabilized the system by simultaneously controlling the differential-mode errors between channels, while simultaneously controlling the total average power output. For three outputs, we define $T_1 = 1$, and then bang-bang control T_k based on the ratio of V_k/V_1compared to the ideal value. T_{k+1} is controlled by value of V_1compared to the absolute target value.

Algorithm 1 Awk script solving the discrete difference equations to calculate startup transient and steady state voltages.

```
awk '
    BEGIN {
        L=100e-6;          # single inductor inductance
        C=1e-6;            # capacitance at each output
        R1=3.16;           # load resistance for 1.0 volt output
        R2=25.0;           # load resistance for 3.3 volt output
        R3=178.0;          # load resistance for 20 volt output

        T1=1.00;           # computed on time for 1.0 volt drive
        T2=0.417;          # computed on time for 3.3 volt drive
        T3=0.355;          # computed on time for 20 volt drive
        T4=0.123;          # computed on time for power supply

        VC=5               # main power supply
        DT=1e-7            # simulation time step

        i=0; V1=0; V2=0; V3=0; I=0          # initialize

          for (t=0; t<.0005; t+=DT) {

                    I+=(1/L)*(VC-V1)*T1*DT;
                    V1+=(1/C)*I*T1*DT;
                    V1-=(1/C)*(V1/R1)*DT;

                    I+=(1/L)*(VC-V2)*T2*DT;
                    V2+=(1/C)*I*T2*DT;
                    V2-=(1/C)*(V2/R2)*DT;

                    I+=(1/L)*(VC-V3)*T3*DT;
                    V3+=(1/C)*I*T3*DT;
                    V3-=(1/C)*(V3/R3)*DT;

                    I+=(1/L)*T4*VC*DT;

                    DD[i]=D; AA[i]=A; II[i]=I;
                    VV1[i]=V1; VV2[i]=V2; VV3[i]=V3;
                    TT[i]=t; i++
          }

        print "title", D, E, F, VV1[i-1], VV2[i-1], VV3[i-1]
        print "xscale 1 [seconds]"
        print "yscale 1 [volts]"

        #for (j=0; j<i; j++) print TT[j], II[j]
        for (j=0; j<i; j++) print TT[j], VV1[j]
        for (j=0; j<i; j++) print TT[j], VV2[j]
        for (j=0; j<i; j++) print TT[j], VV3[j]
    }
'
```

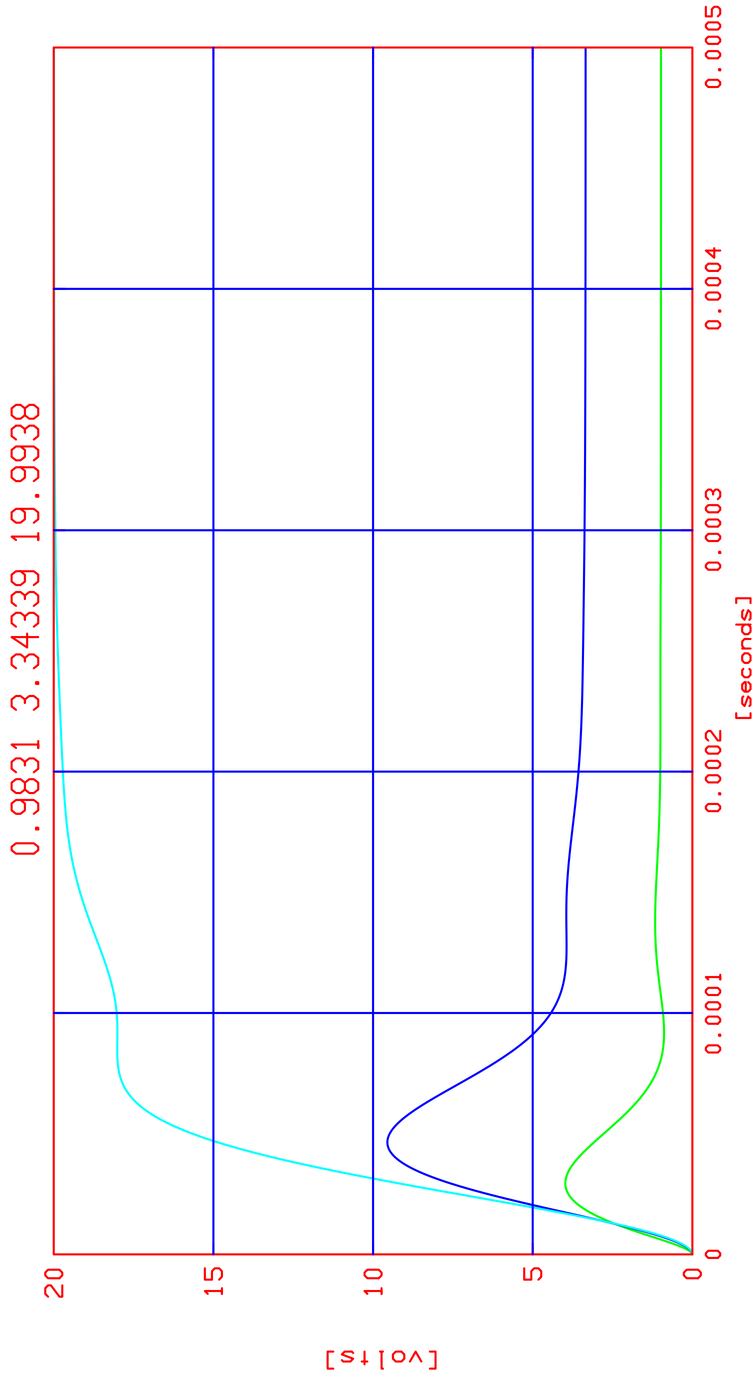

Fig. 1: Simulated power supply start up and final voltages

The difficulty is the interaction between adjustments. It is desired that a step change in current draw on one channel not cause a transient on the other channels. To achieve this goal, it will probably be necessary to create a decoupled control space, so that a change in V1 involves changes in all the timing values, such that the change will be first order cancelled in all channels not equal to V1. This can be certainly done with algebra by embedding the above equations in the control chip, and by measuring the output currents of each channel. It might also be done efficiently with a numerical gradient-based optimizer such as Nelder and Mead's downhill simplex algorithm.